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This grant are to simulate and fabricate an optimized micromachined microject array (MJA) impingement cooling device for high power electronics. A chip-scale microjet impingement cooling device will also be implemented with heat source fabricated on its target plate. There are three main tasks for this project. Task 1 is to develop micromachining processes for the fabrication of the MJA impingement cooling device (Dr. Ang). Task 2 is to obtain an optimized design for the MJA impingement cooling device based on simulation (Dr. Selvam). Task 3 is to apply the optimized device in an application (Dr. Malshe).

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Research Grant No. F49620-00-1-0316

Micromachined Microjet Array Impingement Cooling Device for High Power Electronics

Performance Period: May 15, 2000 to May 14, 2004

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May 31, 2004

Objectives

The objectives of this grant are to simulate and fabricate an optimized micromachined microjet array (MJA) impingement cooling device for high power electronics. A chip-scale microjet impingement cooling device will also be implemented with heat source fabricated on its target plate.

Accomplishments/New Findings

There are three main tasks for this project. Task 1 is to develop micromachining processes for the fabrication of the MJA impingement cooling device (Dr. Ang). Task 2 is to obtain an optimized design for the MJA impingement cooling device based on simulation (Dr. Selvam). Task 3 is to apply the optimized device in an application (Dr. Malshe).

Task 1: Fabrication of MJA Impingement Cooling Devices

Task 1 was performed by Dr. Simon Ang, Dr. Fred Barlow, and their doctoral student K. Saxena. Our main goals are (a) to develop microfabrication processes for the MJA impingement device, (b) to investigate effective bonding techniques for silicon to silicon, (c) to develop a new non-silicon based fabrication technique to reduce the weight and cost of the MJA impingement cooling device, (d) to investigate microfabrication methods to enhance the heat removal capacity of the MJA impingement cooling devices, (e) to develop a low-temperature co-fired ceramic (LTCC) based MJA device, and (f) to design and fabricate a LTCC MJA cooled package and thermal test chip.

(a) Previous MJA Cooler Design

Leland *et. al.* (1999) investigated the first generation of the MJA impingement cooling devices. In Leland's approach, five silicon wafers of 400 microns each were separately micromachined to form the MJA impingement cooling devices. A deep reactive ion etching was performed to etch the piece parts for the MJA cooling device. The five piece parts of the MJA were bonded together using a glue. This approach limited the maximum average temperature of the MJA to about 80°C. The heat source was applied to their MJA cooler using four thick-film resistor heaters soldered directly to a copper heat spreader. Thermal grease was used to minimize the thermal resistance between the copper heat spreader and the MJA cooler. There were 14 T30 AWG thermocouples embedded into the 0.027 inch holes drilled along the midplane of 2.31 mm thick copper heat spreader.

Our Design

In Leland's approach, five piece parts, each of 400 microns thick, were bonded together so that there were four silicon-epoxy-silicon bonding interfaces. This fabrication limitation caused the flow area in the plenum to be slightly restricted at the point where the inlet flow impinges the target plate as well as to turn radially outward due to the insufficient height of the plenum. Our new fabrication technique eliminates the above-mentioned limitation. In our present work, we used three wafers to fabricate the piece parts for the MJA impingement cooling device. As such, we have only two bonded interfaces as shown in Figure 1 when compared to four bonded interfaces as in Leland's MJA devices. As shown, our MJA devices consist of three silicon piece parts of 625 microns thick, bulk micromachined from both sides. This approach reduces the number of bonded interfaces, thus enhancing its reliability and thermal performance.

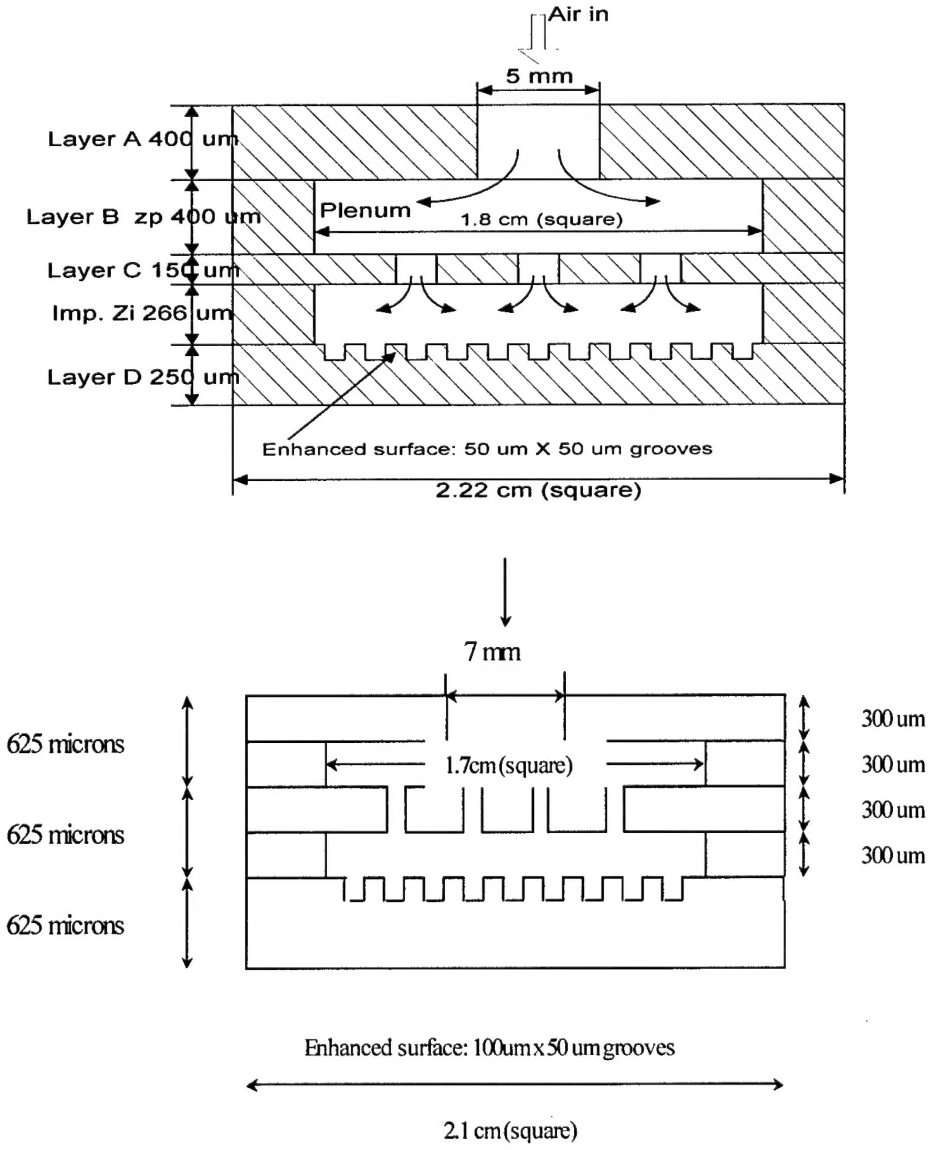


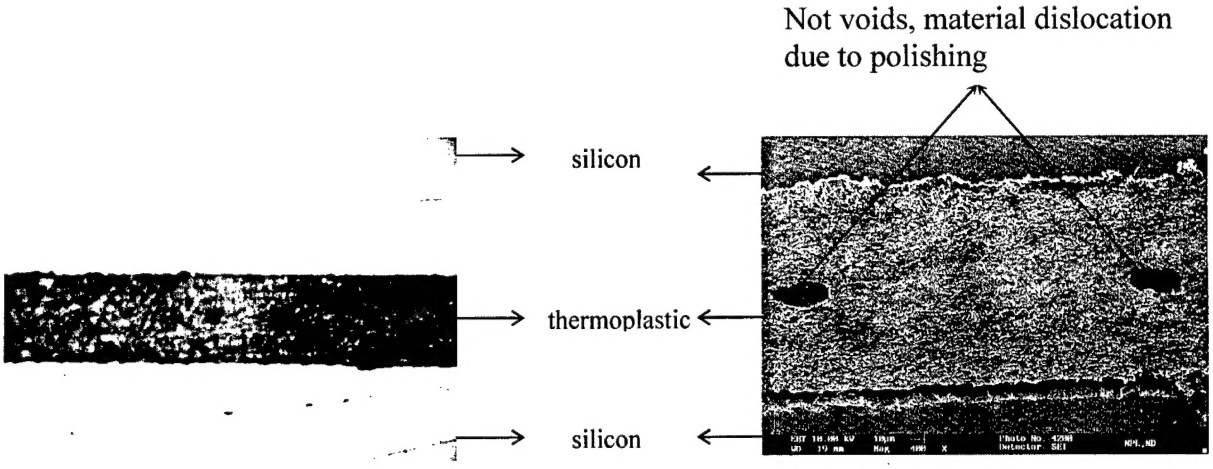
Figure 1: Structural views of Leland's and our present designs.

(b) Silicon-based MJA Fabrication Process

The process sequence for the fabrication of the MJA impingement device is as follows:

a) Cleaning the wafers by SRD (spin rinse dry)
b) Oxide deposition (SiO_2) using PECVD (Plasma-enhanced chemical-vapor-deposition).
c) Metal sputtering (Aluminum in our case).
d) Photolithography.
e) Soft baking and hard baking.
f) Wet etching of the Aluminum.
g) Reactive ion etching.

After complete the above process sequence, the piece parts are bonded together to form the MJA impingement cooling device following dicing. The bonding of the silicon piece parts was investigated extensively. We used a Stay Stik 581.006 thermoplastic material for the bonding. The curing temperature for this thermoplastic is 160-200 °C, which is nearly double the curing temperature for the glue used in Leland's approach. The thermoplastic was cured at 150 °C and 10 minutes in an oven. Figure 2 shows the cross-sectional and SEM micrographs for the silicon/thermoplastic/silicon bond. These bonded structures were subjected to both pull tests and thermal cycling tests.



2(a)Cross-section of the Si-thermoplastic-Si bond 2(b) SEM of the Si-thermoplastic-Si bond

Figure 2. Cross-section and SEM micrograph of the Si/thermoplastic/Si bonds.

Pull tests were performed before and after the thermal shock test to determine the bond strength of the Si-thermoplastic-Si bond. These pull tests were performed

using a Sebastian V pull tester as shown in Figure 3 according to the military standard MIL_STD_883E.

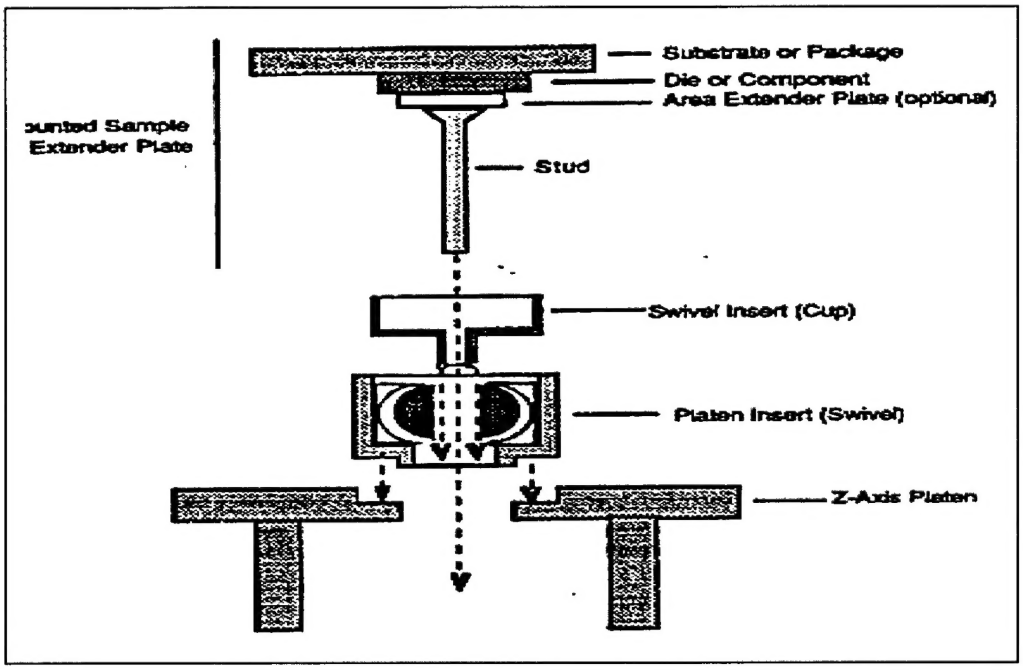


Figure 3. Set up for the pull test.

The bond strength was found to be more than 40-48 kg/cm^2. This was the force at which the JB weld broke, which held the sample to be tested with the aluminum plate but the Si-thermoplastic-Si bond was intact.

Table 1 list the parameters for the thermal shock test.

Parameter	**Set-Point**
Low Temperature	-60 C
High temperature	135 C
Dwell time	2 minutes
Pause time	12 seconds
Number of cycles	20

Table 1. Parameters for the thermal shock test.

In our MJA impingement cooling device, the heater for the heat source and the temperature sensor were fabricated using sputtered aluminum thin film on the backside of the enhanced surface where the air from the micro-jets impinges, i.e., the

heat removing surface for the MJA device. This helps to eliminate the thermal resistances between the heater element and MJA device.

(c) A New Hybrid MJA Impingement Cooling Device

In the present work, we also demonstrated a new hybrid MJA impingement cooling device using a low-temperature co-fired ceramic (LTCC) technology together with a silicon enhanced surface. The plenum and orifice plate were fabricated using the LTCC ceramic. The fabrication of a MJA impingement cooling device using the LTCC technology poses many challenges. There are many advantages of using LTCC. Some of these are: (a) variable plenum height, (b) reduced weight, and (c) reduced cost. The LTCC MJA impingement cooling devices were compared to their silicon counterparts. The results show that both the LTCC and silicon MJA impingement cooling devices have similar cooling capabilities at low input powers.

LTCC fabrication procedures

The LTCC is a glass/ceramic mixture that sinters at less than 900°C. The ceramic substrate and imbedded elements are fired simultaneously, thus giving it the name, co-fired. The LTCC material is composed of glass, ceramic and organic binders. It is usually in the form of flexible sheets known as "green tape". In the fabrication of the LTCC based MJA impingement device, the third part of the device (part with the enhanced surface – the microchannel part) remains to be silicon as the thermal conductivity of the silicon is higher than that of the LTCC. As such, only the plenum and the orifice plate were fabricated using the LTCC.

The main challenge in the LTCC fabrication is the large area cavity, 17 mm X 17 mm. It has been known that the embedded cavities in LTCC will collapse no matter how precisely or efficiently they are designed. One thing that encouraged us to try this LTCC fabrication technique was the fact that we were dealing with the large area but open cavity and not the embedded one.

Since we do not need to do the via filling and printing, the process flow for the LTCC fabrication is as follows:

a) Slitting
b) Preconditioning
c) Collating
d) Prelamination
e) Punching & blanking
f) Laminating
g) Co-firing

Slitting process is accomplished by cutting the ceramic tape, which comes in a roll, into sheets of the size, little larger than the final size of the design. The green tape (Dupont –AJ) was cut from the roll with the dimensions of 6 inches by 5.5 inches. The preconditioning phase was performed in an oven to bake the sheets of tape at 120°C for 30 minutes. Then the layers were collated to obtain the specified thickness for the inlet hole, cavity and microjets. This was performed by stacking the required number of layers, each successive layer being rotated by 90 degree to have an even shrinkage after firing. The LTCC part of the MJA impingement cooling device has three parts to it, inlet hole, microjets, plenum cavity and impingement cavity.

Actually the cavity thickness determines the plenum and the impingement heights for the device. For a better performance of the device, the cavity walls should be straight and there should be no collapse of the cavity walls. Prelamination is a new step that we have introduced as the green tape thickness was small to punch the vias in individual layers and then stacking them together. This step increased the mechanical stability of the layers forming either the cavity or the inlet hole or the microjets. The pre-lamination was performed at the reduced lamination pressures. We used a PTC IL-4008 Isostatic Lamination System, which uses heated water at 70°C water at 1000 psi for 10 minutes to produce a quasi-solid ceramic tape package, devoid of any air pockets. After we had collated and pre-laminated the layers of AJ tape, the inlet hole and microjets were punched using a 20 mil punch. A 12-mil punch was also used to punch the microjets. The via punch step was performed in the PTC APS-8718 Automatic Punching System, producing via holes in the tape. The main challenge in laminating the cavities was the cavity collapse. We did some experiments with higher laminating pressures (2000-3000psi) and the collapse was found in the laminated cavities with the inlet hole layer and the cavity layer. To avoid the collapse, we used lower laminating pressures both for the pre-lamination and lamination after collating cavity layers with the inlet layer and microjet layer. After having laminated and inspected the cavity collapse (which was nearly zero), the firing of the laminated parts of the MJA were performed. The substrate was then placed in the **Fisher-Scientific Isotemp® Programmable Forced-Draft Furnace** for firing. The substrate was placed on a quartz tray and heated in accordance to the co-firing profile as shown in Figure 4 below.

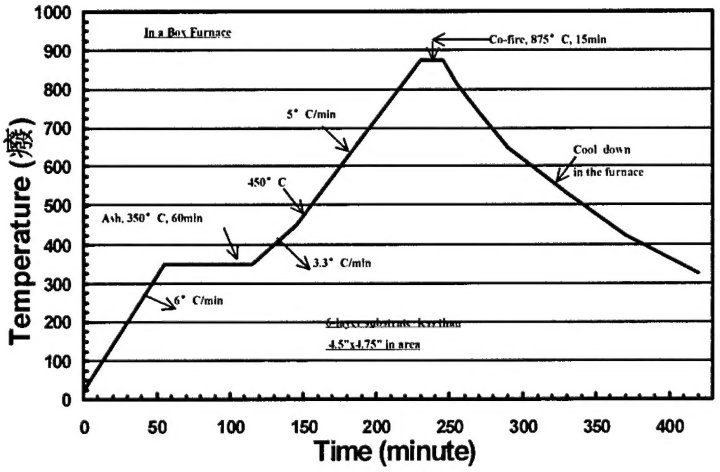
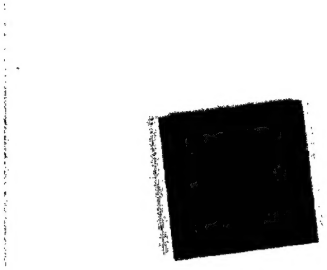


Figure 4. Co-firing profile for the substrates

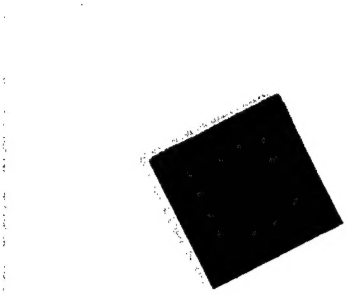
After having fired the LTCC substrates, they were inspected and found to have no collapsed cavity. Another challenge in LTCC processing is due to the fact that prediction of the shrinkage is not trivial and the shrinkage depends upon the type of the LTCC tape used, laminating pressures, embedded materials etc. So in order to

predict the shrinkage more accurately, we did the test sample lamination, firing etc. to get the desired dimensions of the fabricated substrates.

Figure 5 shows the top and bottom views of the fabricated LTCC MJA impingement cooling device. The heater and sensing elements can be clearly seen from the bottom view of the MJA device.



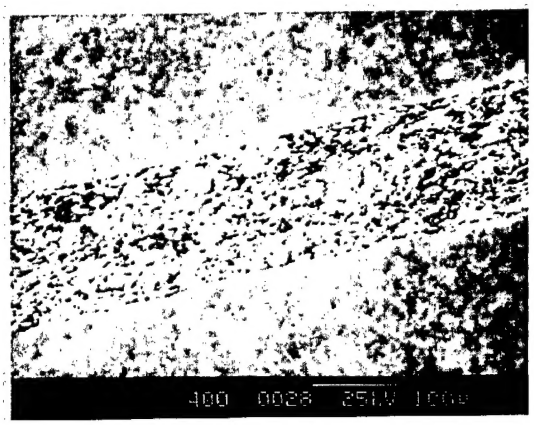
Top two layers of hybrid MJA, inlet hole and microjets in LTCC.



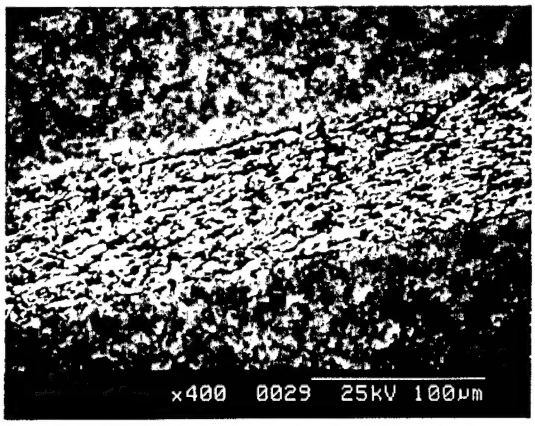
Backside of the third layer of hybrid MJA in silicon

Figure 5. Top and bottom views of the LTCC MJA Impingement Cooling Device.

Thermoplastic epoxy was used to bond the LTCC to LTCC and LTCC to silicon. The bond strength was found to be more than 40 kg/cm^2, similar to those for the silicon to silicon bonds. Again, the LTCC-thermoplastic-LTCC-thermoplastic-LTCC bond was left intact. Figure 6 shows the SEM micrographs of the LTCC-LTCC at a magnification of 400X .



LTCC-thermoplastic-LTCC bond
At 150 C for 10 min cure time

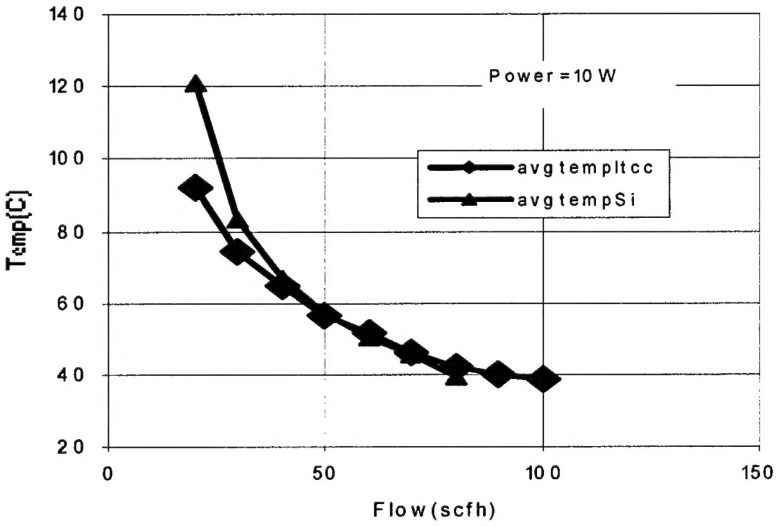


LTCC-thermoplastic-LTCC bond
At 160 C for 10 min cure time

Figure 6. SEM micrographs of the LTCC-LTCC bonds.

(d) Comparison of the silicon and LTCC MJA Impingement Cooling Devices

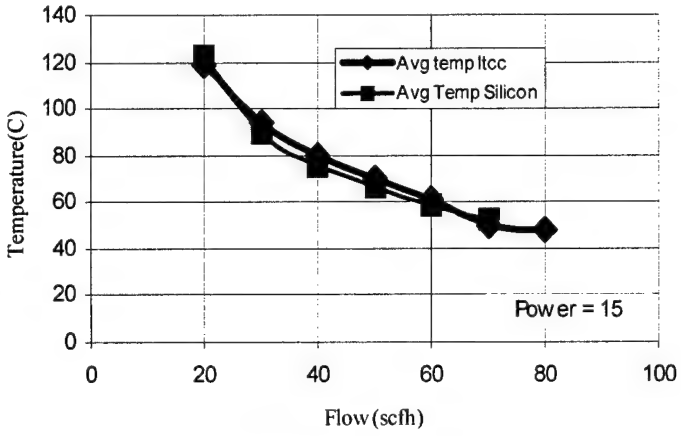
Figure 7 shows the temperature versus air flow at 10W input power for the silicon and LTCC MJA impingement cooling devices. As can be seen, the two plots are very similar to each other.



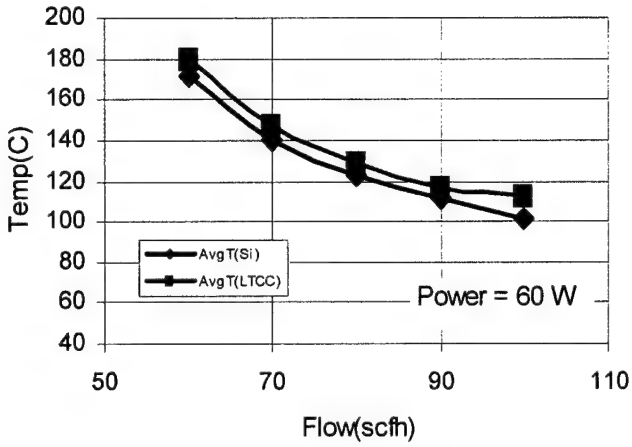
Chip temperature Vs air flow at 10W.

Figure 7. Temperature versus air flow at 10W input power for the silicon and LTCC MJA impingement cooling devices.

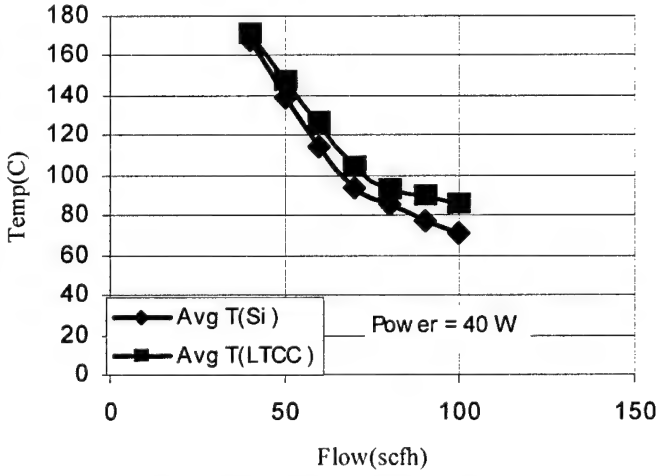
Figure 8 shows the temperature versus air flow at various input powers for the silicon and LTCC MJA impingement cooling devices. As can be seen, the temperatures for the silicon and LTCC MJA impingement cooling devices are quite similar for lower input powers. At higher input power of 70W, the temperature for the LTCC MJA impingement cooling device has a higher temperature than the silicon LTCC MJA impingement cooling device. These results were presented and published at the 2003 International Microelectronics and Packaging Society meeting.



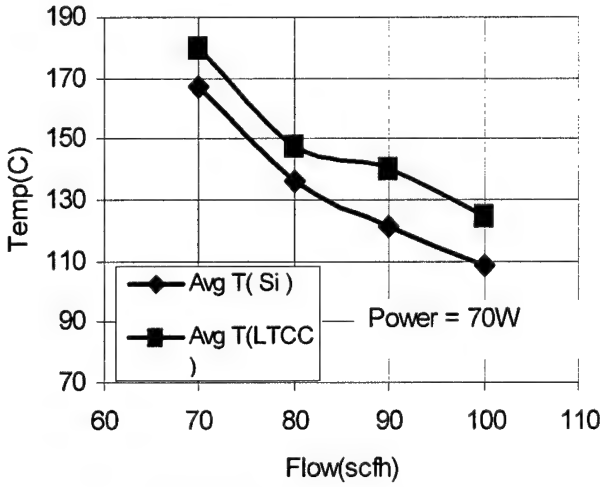
Chip temperature Vs airflow at 15W.



Chip temperature Vs air*flow at 60W.*



Chip temperature Vs airflow at 40W.



Chip temperature Vs airflow at 70W.

Figure 8. Temperature versus air flow for the silicon and LTCC MJA impingement cooling devices.

Temperature measurements were performed on MJA devices and compared to Leland's results. The results are shown in Table 2 below.

Power Density	Flow Rate (g/sec)	Temperature (leland)	Temperature (our)
3.75 W/cm2	0.5	58	47
	0.75	48	36
8.75 W/cm2	0.55	no data	69
	0.75	no data	45
	1	69	40 @0.86g/sec

Table 2.

Figure 9 shows the average surface temperature versus air flow rate for our MJA and Leland's MJA devices. As can be seen, we consistently achieving a lower average temperature on the heat removing surface for our devices when compared to those of Leland's .

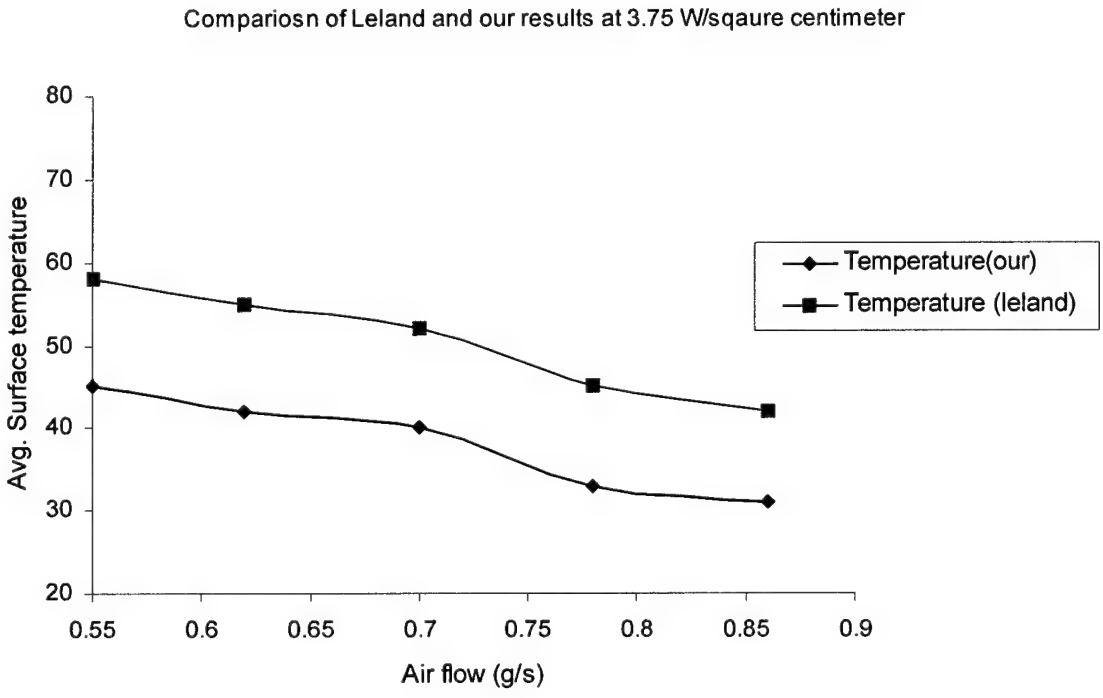


Figure 9. Average surface temperature on the heat removing surface of our MJA and Leland's MJA devices

(e) Enhanced Surfaces for MJA Impingement Cooling Devices

In order to enhance the cooling capacity for the MJA impingement cooling devices, two new surface features were fabricated on the target plates. The first is a lapped surface using 180 grit alumina polishing papers. The surface roughness profile of the lapped surface is shown in Figure 10. As can be seen, streets of 15 microns deep grooves were created on the lapped surface.

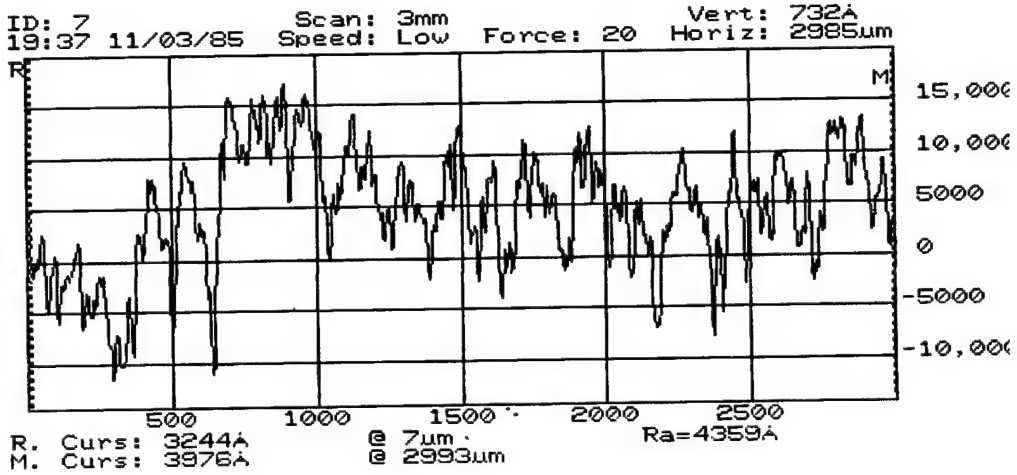


Figure 10. Surface roughness profile for the lapped surface.

Figure 11 compares the heat removing capacities of the silicon MJA impingement cooling devices with micro-channels to that with a lapped surface on the heat removing surface at an input power of 3.75 Watts /cm^2. As can be seen, the temperatures on the lapped surface MJA device is slightly higher that those on the micro-channeled MJA device. There is approximately 5^{o}C difference in the average temperature on the heat removing surface at various flow rates.

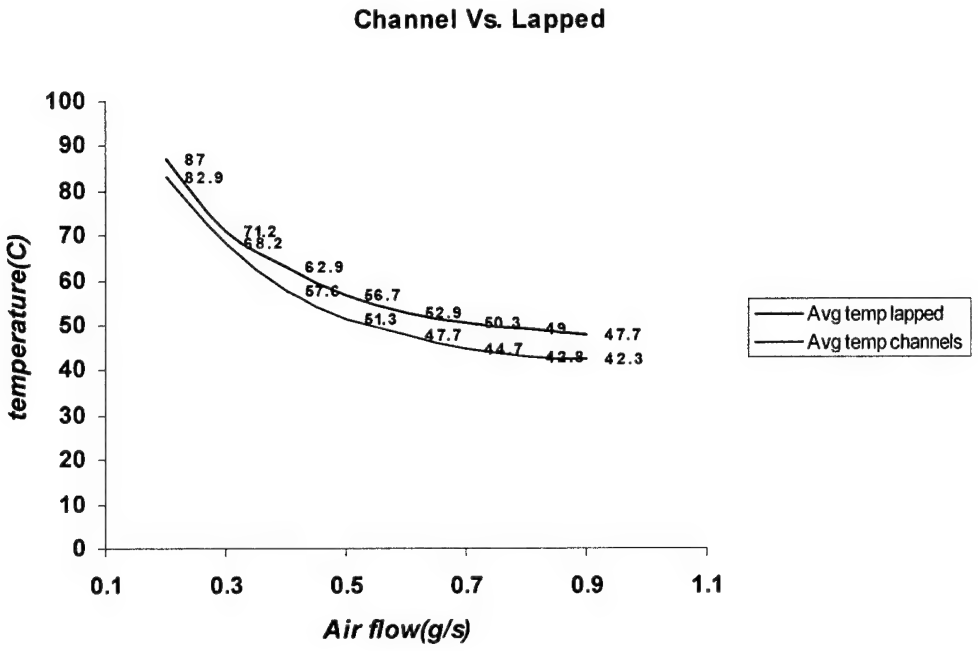


Figure 11. Temperature versus air flow for MJA devices with lapped and micro-channeled surfaces.

We also investigated micro-extrusions on the heat removing surface of the MJA impingement cooling device. These micro extrusions are 50 μm squared and 50 μm deep as shown in Figures12 and 13.

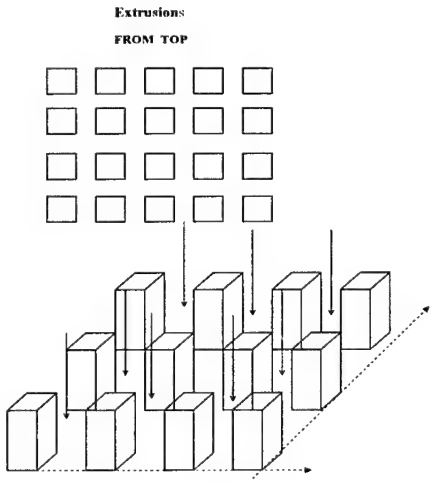


Figure 12. Micro extrusions on MJA device.

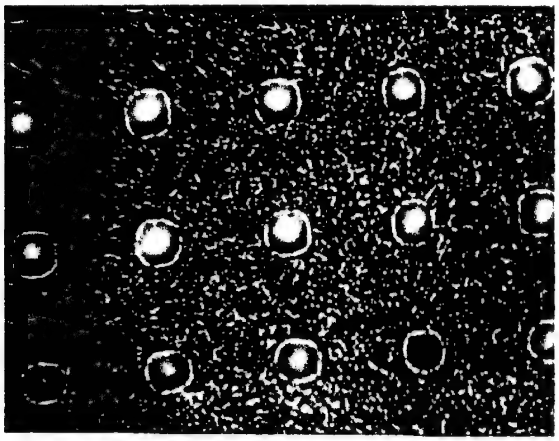


Figure 13. Top view of fabricated extrusions (50um x50 um)

(f) Design of LTCC MJA Cooled Package and Thermal Test Chip

A LTCC MJA cooled package and thermal test chip was designed and fabricated. In this work, these devices have been adapted to create novel IC packages that integrate the traditional packaging functions, device protection and ease of assembly, with effective impingement cooling. These compact packages are ideally suited for high density digital ICs with large power densities, and can be mounted to a printed wiring board and cooled via a compressed air source.

LTCC, which is a glass-ceramic, was selected for this application due to its ability to easily incorporate the three dimensional channels and structures needed for the micro jet array, as well as any desired electrical structures. The technology also offers low loss at high frequencies and other properties that make it desirable for a wide range of electrical applications. In particular DuPont 951 LTCC material has properties suitable for this application, such as fracture strength of 320MPa, thermal coefficient of expansion (TCE) of 5.8×10^{-6}/°C, thermal conductivity of 3.0W/m·K, and insulation resistance above $1 \times 10^{12}\Omega$ (at 100V DC).

The advantages of using LTCC for this application include; it is simple to process, and the availability of multiple tape thicknesses allow designers to easily meet the dimensional requirements for optimum cooling performance. Furthermore, all parts for the cooled package can be co-fired together to form a monolithic device. As a result, long-term reliability can be significantly improved through elimination of the interfaces among the parts that had previously been bonded together in a separate process step. Moreover, this LTCC cooled package protects the IC chip underneath and no additional packaging is needed for the chip.

The LTCC MJA cooled package consists of five sections: inlet, inlet cavity or plenum, micro jet array, microjet cavity and a chip cavity. Figure 14 illustrates a cross section of the package and its various sections. To provide a compressed air input, the researchers used a Delrin block bonded to the top side of the LTCC inlet section. The chip is bonded inside the cavity to form the final package. Since the IC in question is bumped with solder balls the whole package now becomes a MicroBGA that can be soldered to a printed wiring board and under filled.

Design of the MJA cooling section was optimized through numerical modeling performed by Dr. Paneer and his graduate student, Y. Jung. Numerical models of the flow and heat transfer were created to enhance the heat removal capacity of MJA air impingement cooling devices, using the finite difference method . The numerical study provides understanding of the flow features inside the MJA and is a powerful

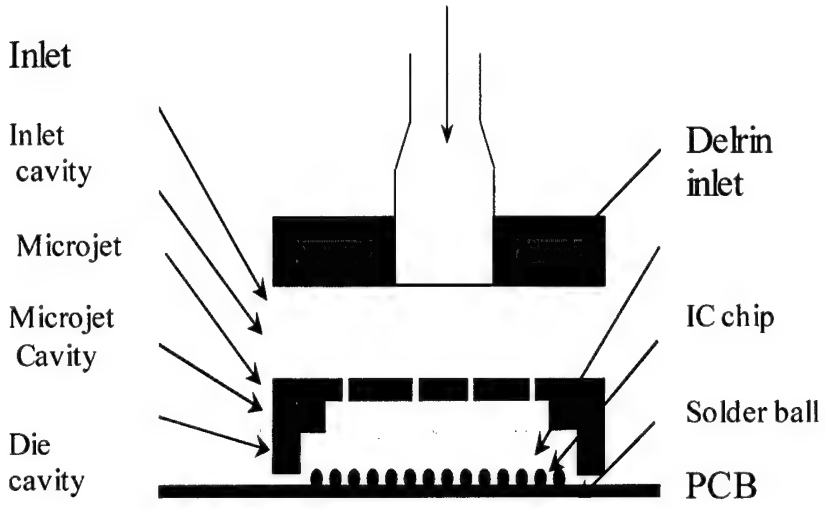


Figure 14. A LTCC MJA cooled package.

tool to improve the heat transfer capacity. The same work cannot easily be accomplished experimentally because of the relatively complex and small geometry of the devices. This work included development of incompressible Navier-Stokes equations for this application. To solve the governing equations, some computational schemes such as the finite difference method and the upwind scheme were applied. Then, computational configuration and grid generation were conducted. The computer modeling is strongly dependent on boundary conditions and their application, so proper boundary conditions were investigated.

To improve heat transfer capacity and find the optimum configuration, different grids were made to cover all of the jet parameters studied. By changing the parameters of the microjet array, shown in Figure14, such as distance from the jet to the IC, Z, jet diameter D, jet spacing Xn, plenum height H_1, and length of the jets H_2, various configurations were investigated. Impinging height ratio Z/D and jet spacing ratio Xn/D were also investigated. An optimum configuration based on the numerical modeling was used to fabricate the LTCC MJA air impingement packages.

In order to experimentally evaluate the heat dissipation performance of the LTCC MJA cooled package, a 125 mm Si wafer of thermo-mechanical test chips, one of which is shown in Fig. 15 were designed and fabricated to simulate an integrated circuit. The first step in this process was to wet-etch micro-channels on the backside of a silicon wafer to increase the surface area that the air impinges upon. Then, a copper thin film was sputtered on the front side of the wafer, patterned and etched to form nine heating elements (heaters) and nine temperature sensors. Once the heating and sensing devices were completed, the silicon wafer was diced into the desired test chip size. As can be seen in Figure15, the heaters at the top two corners have single heating elements whereas the rest are composed of a pair of identical heating elements. Each pair was connected in parallel in order to uniformly spread the power loss over the surface area of the test chip.

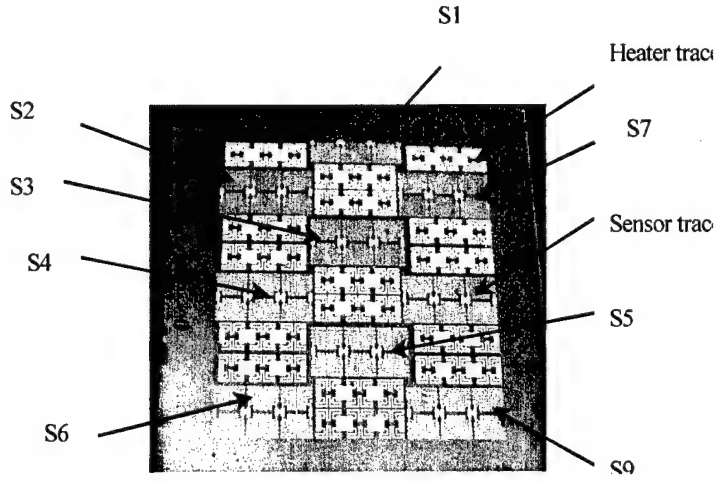


Figure 15. A thermal test chip.

Fabrication of LTCC Microjet Array Cooled Packages

LTCC is a glass/ceramic that sinters at less than 900°C. The ceramic substrate and any embedded electrical circuits, which are comprised of metal traces and vias, are co-fired simultaneously. For the LTCC based MJA cooled package, the micro channels are located on the back of the silicon device to be cooled, the silicon die or active device is flip chipped on the printed circuit board. The inlet and the microjet array and the die cavity are all fabricated from LTCC material. The cavity encloses the thermal test chip providing mechanical support and the depth of the cavity determines the impingement distance.

DuPont 951 LTCC was used to fabricate the LTCC microjet array-cooling package. Since each of the five parts for the LTCC package comprises multiple layers, delamination between tape layers under or over the inlet hole, micro jet and die cavities must be avoided. Fabrication of cavities with the normal lamination pressures

recommended by the material manufacturer, tend to collapse the LTCC material over or under the cavity area, resulting in a concave rather than a flat substrate. Therefore, some preliminary tests were carried out to resolve these process issues. It was found that pre-lamination of LTCC layers helped eliminate delamination of layers and the combination of a particular fixture and low lamination pressure produced a flat substrate.

The LTCC process begins with slitting the flexible green tape from a tape roll to desired size: 6"x5.5" to fit the tooling used for this particular application. After the tapes were preconditioned at 120 °C for half an hour, the desired number of tape layers for each part was pre-laminated under a particular pressure, temperature and time. Designs for the inlet, cavity, microjet array and die cavity were then formed using a mechanical punching system. Afterwards, the punched tape layers were stacked and laminated under a controlled process conditions. Firing of the laminated LTCC substrate at a temperature of 875°C for 15 minutes turned the green tape materials into a robust ceramic. Four packages in a fired LTCC panel were finally diced into the desired dimensions. At this stage, a LTCC microjet array cooled package is ready for assembly.

This fabrication process has a number of advantages such as

- The ability to create variable plenum heights.
- Reduced overall weight.
- Reduced fabrication complexity.
- Potential for increased reliability.
- Integration at the board level.
- Reduced cost in comparison to silicon based technologies.

The main challenge in the fabrication is the large area cavities, which are 17 mm by 17 mm in this particular design. It has been found in previous work that the embedded cavities have a tendency to collapse unless special process conditions are imposed. For the design discussed in this paper a large area but partially open cavity is required.

Test Setup and Procedure

As shown in Figure 16(a), the package consists of a LTCC MJA, a PCB test board and a thermal test chip between them (invisible in the top view). Through the LTCC package, air impingement cooling is applied onto the backside of the thermal test chip to be cooled where micro channels were wet-etched to increase the cooling surface. Heating elements and temperature sensors were directly fabricated on the front side of the test chip and flip-chip bonded onto the PCB test board using solder balls of 0.2mm (8mil) in diameter. For the sake of reliability, flip chip under-filling was performed once the thermal test chip was bonded to the PCB board that provides interconnect to the temperature sensors and heating elements. Power planes were located on the bottom of the board. Through holes in the PCB board also act as

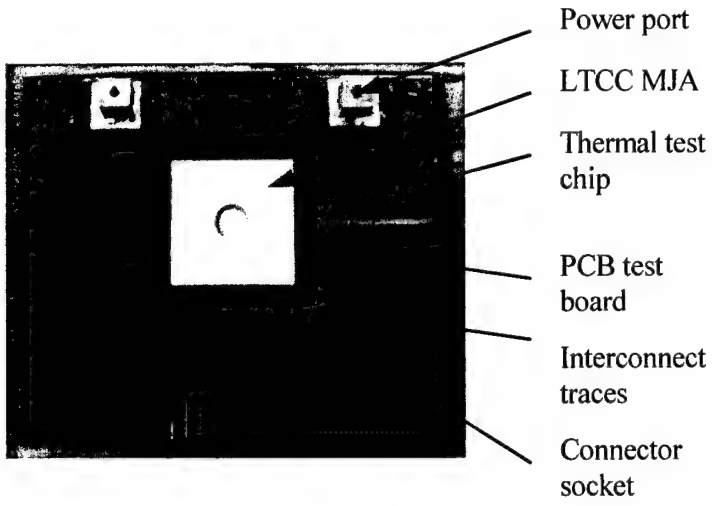
connections for the power planes and the two power ports soldered on the top through which the DC power is applied to the heating elements on the test chip.

The measurements were conducted by varying the applied airflow at different power levels. The test set up is shown in Figure 16(b). A HP4263A LCR meter in four-probe contact mode was utilized to measure resistance of each temperature sensor and then the resistance was converted to temperature according to the temperature coefficient of resistance (TCR) from a calibration that was performed prior to the cooling test. The temperature accuracy of this method is ± 0.2°C. An eighteen channel switch box was used to connect multi-point switch connected the HP LCR resistance meter and the connector socket on the PCB board through a 37-pin ribbon cord as we used 36 pins for nine sensor, using four-probe contact method. By simply switching the inputs designed for each of the nine sensors, resistance value of each sensor can be quickly acquired under the same testing conditions. It should be noted that the four-probe contact method eliminated resistance of interconnect traces on the PCB board and wires between the meter and the ends of a sensor and, thus, only the resistance of sensor itself was measured.

The compressed air was introduced through the inlet of the MJA package with the DC power applied at a constant current. The current was varied from 0.25 Ampere to 2 Ampere, while monitoring the maximum current value corresponding to the highest sensor resistor value at 100 °C. This was the limit for the power applied. The current was varied at each airflow value, over an air flow range from 20 scfh to 70 scfh. From these measurements, the variation of average chip temperature, which is the temperature averaged for the sensors, with airflow were made at different power levels. Also the graphs of the highest chip temperature sensors with varying airflow and for the lowest chip temperature sensors with varying air flow at different power levels were plotted. For this purpose the average power was taken, as the measurements were done with the constant current. So we obtained the average power values of 0.8, 3.3, 7.8, 14.3, 23.7, 35.7, 46.6 and 68 watts with the maximum standard deviation of 2.6 watts, which was ± 7.31% and with the minimum deviation of 0.02 watts, which was ± 2.54%.

Experimental Results

Figures 17, illustrates the variation of the average device temperature with the amount of power applied to the thermal test chip at different airflow values. From the graph, we can see that at low airflow values, the slope of the graph is steep, which indicates that there is a large change in the average chip temperature with a small change in the power applied to the chip. This trend indicates that the chip is heated more rapidly than the heat can be taken away by the air at these low flow rates. As the airflow increases, we see that the slope of the line decreases, meaning that for the same variation of power, the temperature change is small for the higher flow rates. This device is able to effectively remove 68 watts of power loss, which corresponds to 15W/cm^2 at 70 scfh, with the average chip temperature no more than 102 °C.



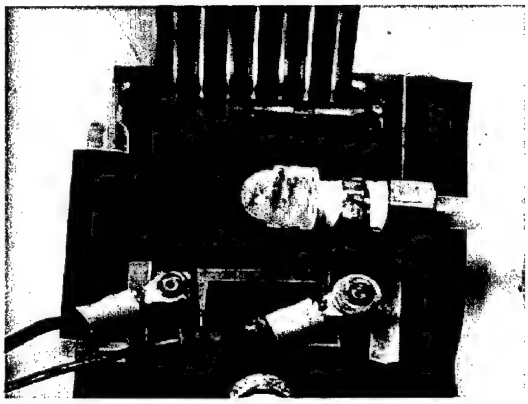


Figure 16. (a) A LTCC MJA cooled package, (b) test set-up.

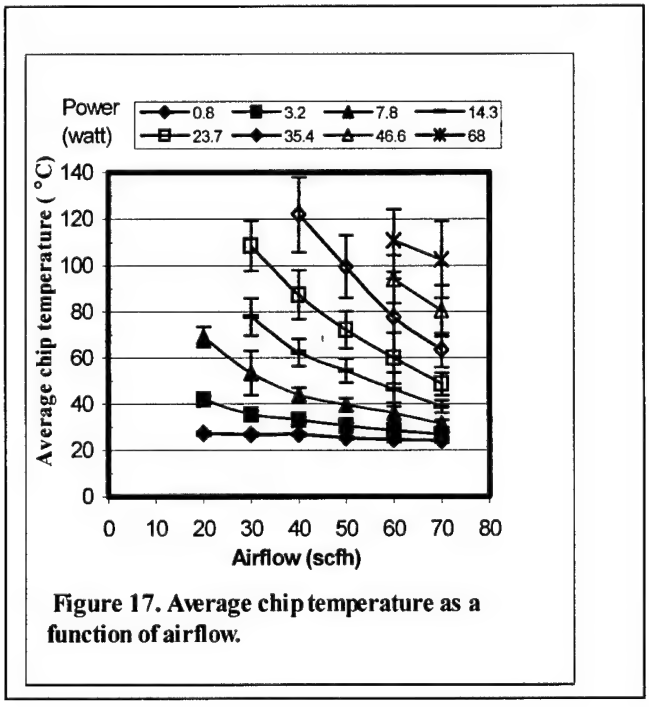


Figure 17. Average chip temperature as a function of airflow.

Figure 18 illustrates the variation of the average chip temperature with increasing air flow at different power levels. At the lower power levels, there is not much change in the chip temperature with the increase in the airflow; this means that we do not require higher airflows at low power levels to cool the IC as expected. But at higher power levels, there is a large change in the average chip temperature with a corresponding change in the airflow, which indicates that at higher airflows the device is sensitive to variations in the air supply.

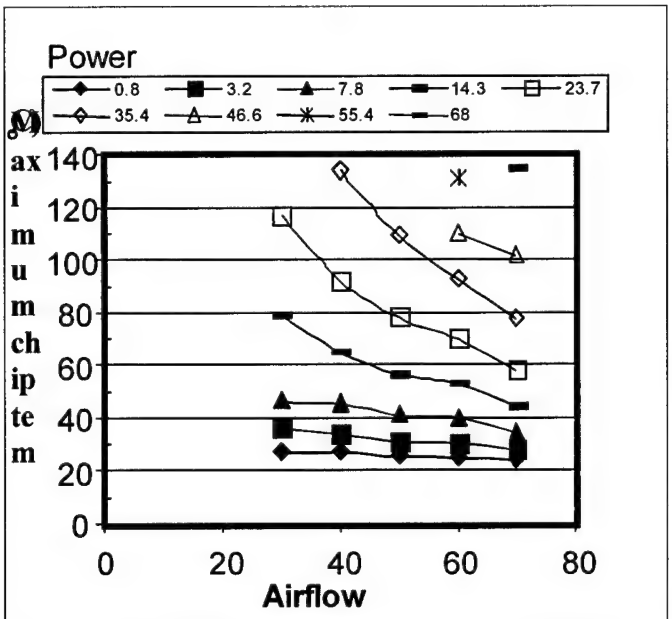


Figure 18. Maximum chip temperature versus airflow.

Figures 19 and 20 plot the data for the sensor that showed the maximum chip temperature, and the sensor, which showed the minimum chip temperature, at different airflow values. This gives an idea of what were the temperature ranges on the chip as it was cooled. These graphs were plotted at different power levels. For example, at the power level of 35.41 watts and at airflow of 50 scfh, the maximum temperature on the chip was 120°C, the minimum temperature was 85°C. This variation of temperature was due to the design of the thermal test chip and does not reflect a lack of uniformity in the MJA cooler. The heater elements are connected in series and spread out over the chip area. The heaters are all identical except for the top two elements, which dissipate twice the power of the other heating elements. The sensor elements are also distributed over the chip and are labeled in Figure 15 as S1

thru S9. These sensors see different heating conditions. For example, S1 would be the maximum temperature as the two high resistance heaters surround it, having double the resistance as compared to the rest of the heaters on the chip. Similarly the sensors, S6 and S9 will see the same heating conditions as they are surrounded by two similar heaters.

As we report this work, efforts are underway to test the performance of the MJA cooling package at higher air flow rates. Nevertheless, if we extrapolate the graph in Figure 20, keeping the average chip temperature within the safe operating limits (in our case, we have assumed 80°C) we are able to identify the critical values of power at a particular airflow. Also from this extrapolated data, we are able to predict the amount of power that we could apply to the IC within the safe limits of operation at higher flow rates. It can be seen that the device can support power losses up to 86.8 watts for a flow rate of 90 scfh for a maximum device temperature of 80 °C, which corresponds to a power density of nearly 20W/cm^2. Similarly at 150 scfh and a maximum device temperature of 80 °C, the device can support 133 watts of power loss corresponding to a power density of 30W/cm^2.

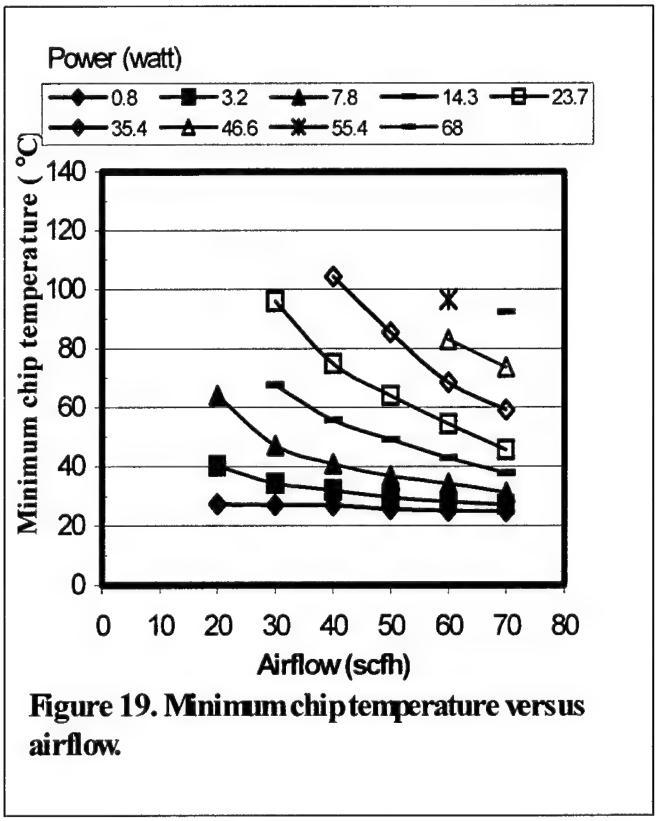


Figure 19. Minimum chip temperature versus airflow.

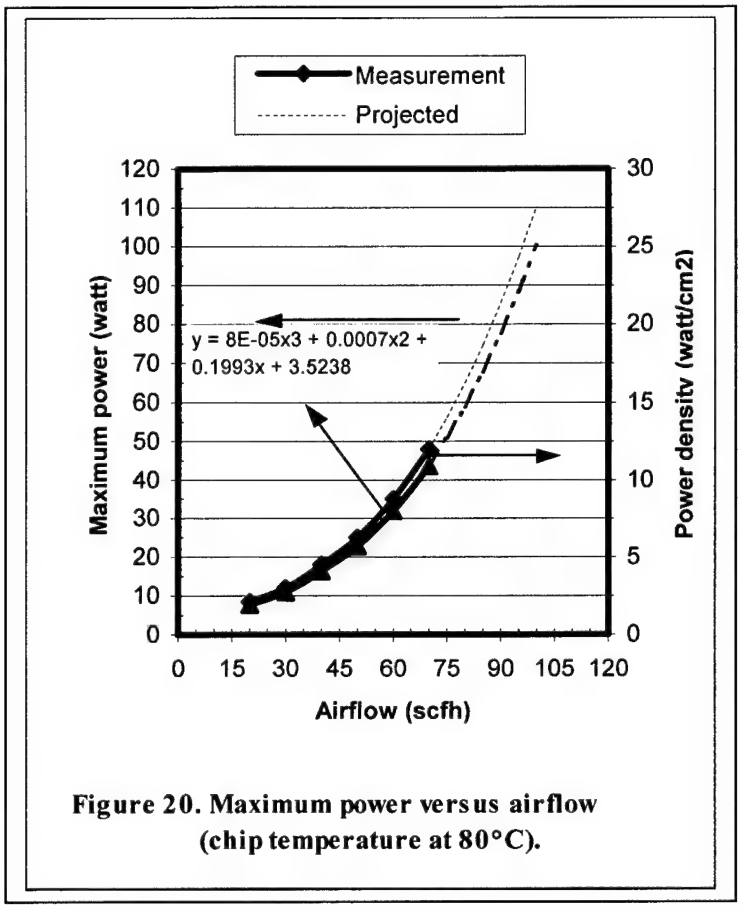


Figure 20. Maximum power versus airflow (chip temperature at 80°C).

Summary

In the present work, LTCC MJA cooled packages have been designed and fabricated. The optimum parameters were used for the plenum height, impingement height, jet diameter, jet spacing, jet length as determined from numerical analysis of the micro jet array. This package can directly cool the IC chip on the printed circuit board without encountering any other thermal resistances associated with the package. No other packaging is required for the IC chip using the cooled package as it does both the jobs of a conventional IC package and as well as the thermal management solution.

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[1.6] Saxena, K., Wang, G., Ang, S., Elshabini, A., Barlow, F "LTCC based MEMS impingement coolers" Proceedings of SPIE - The International Society for Optical Engineering, v 5231, 2003, p 211-216.

Task 2: Simulation of an Optimized MJA Impingement Cooling Device

The simulation task of this project was performed and reported by Dr. Paneer Selvam and his doctoral student Y. Jung.

This research is concerned with the development of a finite difference program to analyze the heat removal capacity of a micro-jet array using viscid incompressible and compressible flow models. Numerical results were compared to experimental values as a bench mark for accuracy. This study focused first on development of a three-dimensional computational model that would be in agreement with experimental results. Then using this model changes in the micro-jet array were implemented to improve its cooling capacity. Next a two-dimensional computer model using compressible flow was developed for the initial array configuration. Once the boundary conditions using this model are optimized then a three-dimensional model is being produced. Currently this is the focus of this study.

The first part of the incompressible flow research involved developing a three-dimensional computational model that accurately predicted the cooling capacity of the micro-jet array. Grids using 381,000 to 1,350,000 grid points were used in an attempt to optimize the number of points used, and keep computational time and memory requirements to a minimum. This goal was met and computational results were in good agreement with the experimental results of Leland et al. (1999). This research was published in ***the Second International Symposium on Advanced in Wind and Structures***.

The next step in this study of incompressible flow was to optimizing the characteristics of the micro-jet array used in the analysis. This optimization focused on changing the geometry of the micro-jet array to improve its cooling capacity. Variations applied to the micro-jet array configuration include using different jet spacing, number and size, and changing the height of the plenum. Application of geometry changes to the micro-jet array using the computational model led to increasing the cooling capacity of the array by 78%. These results were published at ***2001 International Symposium on Microelectronics.***

Then a computational model was developed for two-dimensional compressible flow using the original micro-jet array. This part of the research used two-dimensional flow to model the array in an effort to minimize computational resources while boundary conditions are developed. This goal was achieved when the computational results were again in good agreement with Leland et al. (1999). These results were published in ***Second International Conference on Fluid Mechanics & Fluid Power***. Further research using two-dimensional flow produced yet closer agreement with experimental results due to the development and application of more accurate boundary conditions. Publication of these results is pending.

Now that accurate boundary conditions have been established, a three-dimensional compressible flow computational model is being developed. The results from this study will also be compared to Leland et al. (1999) as a bench mark for accuracy and array optimization will follow as outlined above for two-dimensional flow. Publication of this research will follow.

(b) Three-dimensional Computer Modeling with Incompressible Flow

The incompressible flow research involved developing a three-dimensional computational model that accurately predicted the cooling capacity of the micro-jet array. This goal was met and computational results were in good agreement with the experimental results of Leland et al. (1999). This research was published in the Second International Symposium on Advanced in Wind and Structures.

The micro jet array (MJA) cooler is shown in Fig. 21. Air enters the device plenum and is distributed over the orifice plate. The air then flows through the orifice plate creating a high heat transfer zone under each of the 221 jets. Then, the air is exhausted from two opposite edges of the cooler. More details about the MJA are given in Leland et al. (1999). Only one quarter of the MJA is considered for computer modeling due to symmetry in the horizontal plane. A computer program is written to generate a grid for this complex region. The grid has 324,000 ($90\times90\times40$) points. In the vertical direction, an equal spacing of 0.025 mm is used. In the horizontal direction unequal spacing is used to consider the hole and no-hole regions of the plate. The diameter of the hole in the orifice plate is discretized using 5 points.

The computed velocities and temperature are visualized. The computed temperature distributions at the bottom of the plate are shown in Fig. 22 and 23. The maximum temperature computed in the solution region is 124°C. As seen in Fig. 22, the temperature near the exhaust is computed to be about 98°C. However, this high temperature will not exist in the experiment. In the computer modeling, the micro-jets in the orifice plate close to the exhaust are not considered, because these holes are very close to the outflow region. Therefore, it will be very hard to solve the equations accurately having such a complex flow close to the outflow region. Also, in reality heat can dissipate by convection and radiation at the edges, but these factors are not considered in the computer model. Hence, for comparison, temperature at the edges is neglected. In the experiment conducted by Leland et al. (1999), they measured the temperature at 16 points. Leland averaged the 16 points and reported the temperature to be about 57° C. It is shown in Figure 16 that right below the micro jets, the computed temperature is below 55° C and it agrees well with the experimental measurement of Leland et al. (1999).

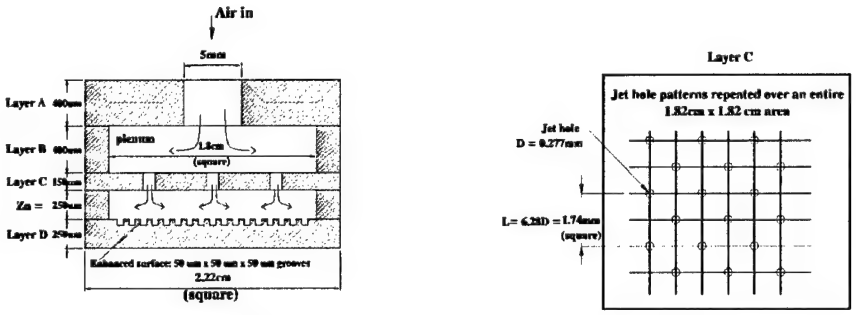


Fig 21. Schematic of micro-jet array cooler

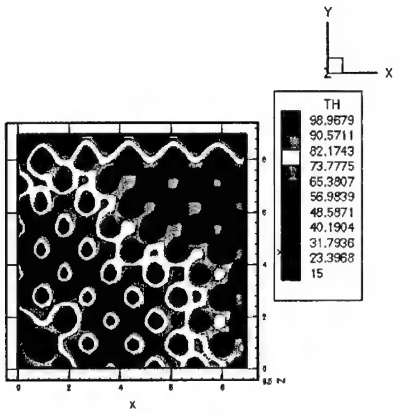


Fig 22. Contour diagram for temperature at the bottom of the plate.

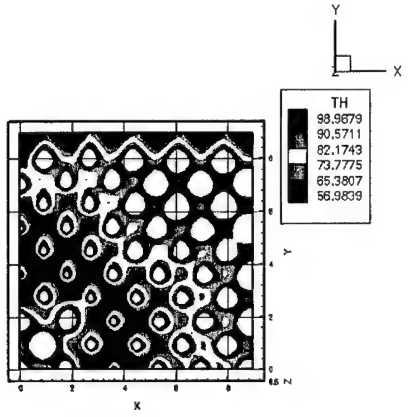


Fig 23 Contour diagram for Temperature above 55° C.

This phenomenon can be explained by visualizing the temperature contours and velocity vector diagrams in Fig. 24 to 26. In Fig. 24, one can see the spread of the hot spot in the vertical direction along the centerline. Fig. 25 shows the re-circulation regions between the second and third hole and between the third and fourth hole from the center. The close up view of the re-circulation region between the second and third hole is shown in Fig. 26. From this illustration, it can be concluded that the re-circulated air retains the heat in those regions and hence a higher temperature distribution is formed at the bottom plate. This phenomenon may be very hard to measure or visualize in the experiment due to the small geometry. Hence, numerical modeling has proved to be a useful tool to understand the flow phenomena.

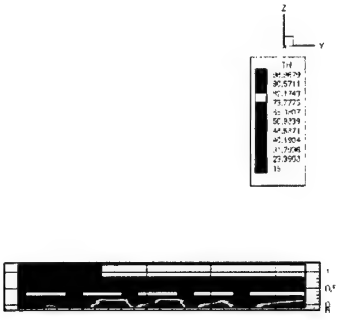


Fig 24. Contour diagram for temperature along the centerline at the exhaust.

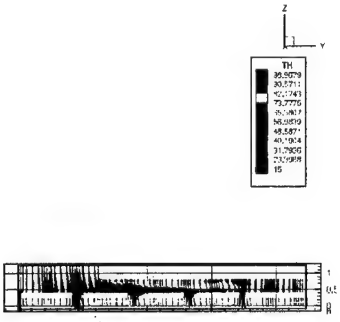


Fig 25. Velocity vector diagram along the centerline.

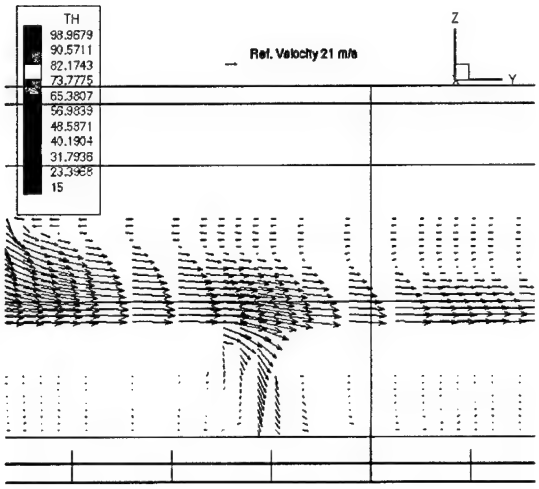


Fig 26. Close-up view of velocity vector diagram along the centerline at the exhaust around the third hole from the center.

(c)_ Optimization of the Heat Removal Capacity

The main objective of the chapter is to optimize cooling capacity of the MJA assembly by modeling the flow and heat transfer in the MJA, using finite difference. The different geometric parameters have been varied to find optimum MJA configuration. Application of geometry changes to the micro-jet array using the computational model led to increasing the cooling capacity of the array by 78%. These results were published at 2001 International Symposium on Microelectronics.

Computational Grids and Boundary Conditions

The different grids used, are illustrated in Table 3 along with all the other boundary conditions and geometric properties used.

Case Number	Description	Parameter Covered
Case 1	W/t layer C	Single jet
Case 2	W/t layer C fewer grid points	
Case 3	Standard Case, D= 0.277 mm, W/t E H, Af = 0.04, .zi/D = 0.96, zp = 0.4 mm	Different jet sizes D with the same Af, zi/D, and zp
Case 4	D= 0.1933 mm	
Case 5	D= 0.1933 mm w/(E H)	
Case 6	D= 0.434 mm	
Case 7	D= 0.277 mm	Af = 0.08
Case 8	D= 0.1933 mm w/(E H)	
Case 9	D= 0.434 mm	
Case 10	Standard Case	Different input velocities

Case 11	Standard Case	
Case 12	D=0.1933 mm w/ (E H)	
Case 13	Zi/D =0.5	Different impinging height ratio zi/D
Case 14	Zi/D =1.5	
Case 15	Zp= 0.3 mm	Different Plenum height zn
Case 16	zp= 0.6 mm	
Case 17	D = 0.1933, Af =0.04 w/ (EH), zi/D= 0.5 zp=0.6	Combination of the best parameters

Table 3: The parameters investigated

Results

All the cases covered are compared to each other by plotting their heat distribution at the top of the bottom plate. The results are shown in Table 4. Figures 27 and 28 show respectively the results achieved by the Standard case (case 3) and the best results obtained in case 17. As seen in Table 4, case 17 is much better than stand case (case 3). Case 17 led to increasing the cooling capacity of the array by 78%. Also it is shown that the smaller Af, smaller jet hole and smaller zi/D, increase the performance. However, because case 17 has larger grid size than case 3, case 17 has much worse convergence.

Case #	Max Heat °C	Avg Temp °C	$\bar{h}$ W/m^2 K	D Avg $\overline{Nu_D}$	Avg imp. $\overline{V_e}$ m/s	D Avg $\overline{\mathrm{Re}_D}$ No	Max exit V m/s	Location X Y Z in mm Of Max. V
1	165	79	463	77	21	4950	47	2.07X2.77X0.075
2	211	89	392	65	21	4946	37	2.275X1.82X0.0625
3	86	49	932	8.6	29	382	90	0.939X0.939X0.225
4	89	42	1264	8.1	37	344	99	1.26X1.26X0.162
5	78	44	1129	7.3	34	318	96	0.60X2.97X0.36
6	120	48	970	14	38	794	92	0.217X2.821X0.58
7	129	67	579	5.3	16	208	79	2.999X0.544X0.45
8	123	65	604	3.9	19	171	85	0.905X0.905X0.162
9	158	75	500	7.2	19	399	82	0.217X2.505X0.600
10	88	51	884	8.2	27	355	78	0.939X0.939X0.225
11	83	48	993	9.2	32	416	106	0.939X0.939X0.225
12	77	41	1270	8.2	40	366	115	0.604X2.972X0.360
13	75	47	1014	9.4	29	377	87	0.8697X2.54X0.300
14	87	50	910	8.4	29	385	91	0.939X0.939X0.35
15	119	55	773	7.1	28	373	104	2.36X1.305X0.45
16	86	45	1113	10.3	30	402	77	0.939X0.939X0.225
17	61	37	1603	10.3	39	361	76	4.181X0.604X0.270

Table. 4 Results

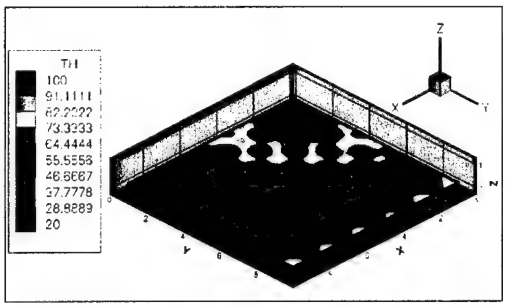


Fig. 27. Stand case (case 3)

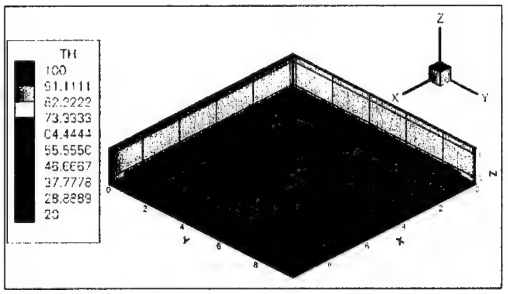


Fig. 28. The best case (case 17)

(d) Two-dimensional Computer Modeling with compressible Flow

When the inlet jet velocity is higher than about 20 m/s, the highest velocity in the micro jets is more than 100 m/s, and the flow is becoming compressible, so incompressible flow modeling from Selvam et al. (2001) and Jung et al. (2002) is no longer applicable. Therefore, when the inlet jet velocity is higher than 20 m/s, the compressible flow should be considered. In this work, two dimensional compressible flow Navier-Stokes equations are considered as a start.

Computational grid and boundary conditions

This goal was achieved when the computational results were again in good agreement with Leland et al. (1999). These results were published in Second International Conference on Fluid Mechanics & Fluid Power.

A nonstaggered rectangular grid system is used in this work. All variables are solved at the nodes. The two-dimensional micro jet array (MJA) cooler is shown in Fig 29. Air enters the device plenum through the inlet jet whose diameter is 5mm and is distributed over the orifice plate. Then the air flows through the orifice plate which creates the high heat transfer. Then, the air is exhausted from two opposite edges of the cooler. In the horizontal direction, unequal grid spacing is used to consider the hole and no-hole regions of the plate. The diameter of the hole in the orifice plate is discretized using 5 points. This grid spacing is smaller than the other regions in the horizontal direction.

The half model in the x-y plane is shown in Fig. 30 because of symmetry of the model.

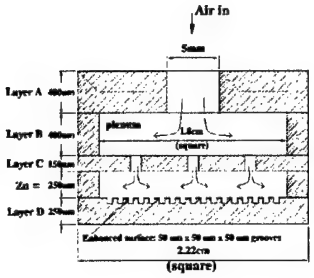


Figure 29. Schematic of micro-jet array cooler

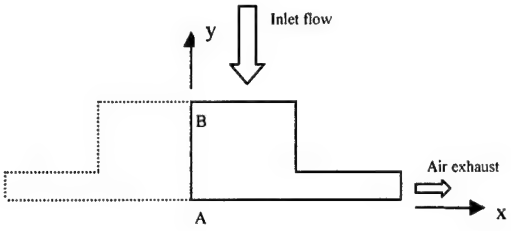
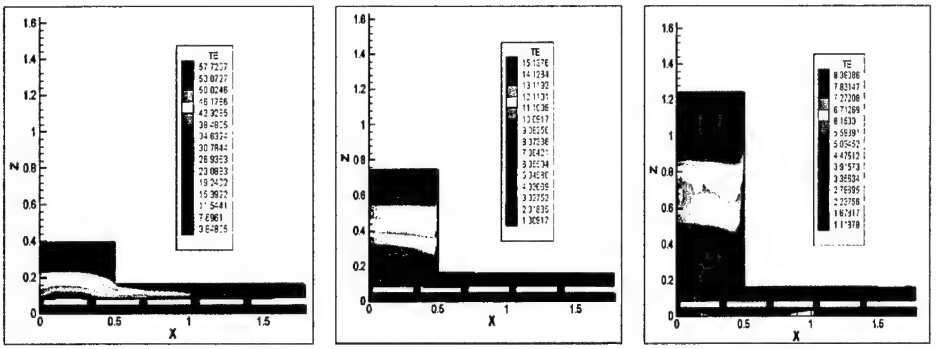


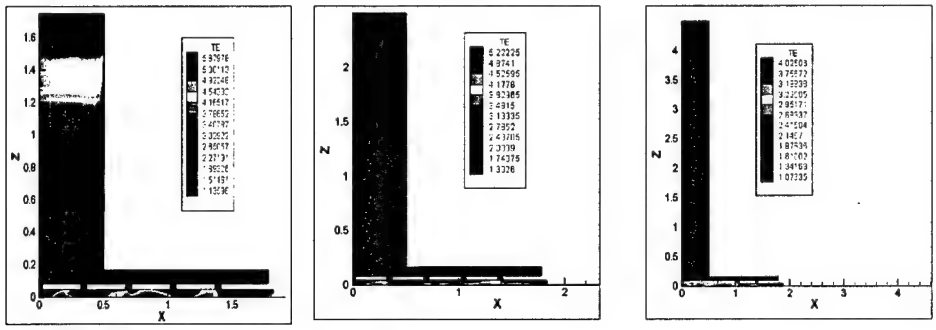
Figure 30. Solution region of two-dimensional micro-jet array

Results and discussion

The micro jet array (MJA) described in the previous section is computed for an inlet velocity of 140 m/s and an input power of 15 W at the bottom of the MJA. The temperature distributions at the jet are shown in Fig.31. Figures 31-a and 31-b indicate that the non-dimensional temperatures at the inlet jet are about 50 and 15, and they are very high temperatures. However, the non-dimensional temperature at the inlet jet must be 1, because it is selected as reference temperature. This may be due to the pressure of inlet very close to the plenum. Here the spacing is varied to study the effects of inlet heights. In Figures 31-a and b, the heights of the inlet jet are shorter than the other models shown in Figures 31-c, d, e and f. This results in higher temperatures in the inlet jet region. When the height of the inlet jet is not enough and the velocity of the inlet jet is very high, the flow and temperature at the inlet jet are affected by whole MJA region, so it is no longer free stream flow region. That is the reason the temperature at the inlet jet is more than 1. Fig. 31-c, d and e show that the height of the inlet jet is increased to 3.11, 4.36 and 6.24cm. Even though the non-dimensional temperatures at the inlet jet are still higher than 1, these models produces better results than the previous models shown in Figures 31-a and b. Figure 31-f shows that the non-dimensional temperature at the inlet jet becomes approximately 1 when the height of the inlet jet is11.24 cm. With this change, the inlet jet region becomes the free stream region. Therefore, it is concluded that when the height of inlet jet is small and the velocity of the inlet jet region is high, the flow is no longer free stream flow. The heights of the inlet jet, the non-dimensional temperatures at the inlet jet and the average temperature at the bottom plate are shown in Table 5. As shown when the inlet jet height is 11.24 cm, the average bottom temperature is 1.83. The non-dimensional average temperature at the bottom is expected to be 1.4 from Leland et al. (1999). The difference in our results may be due to unsuitable boundary conditions. Currently further study is presently being conducted applying the proper boundary conditions. Fig. 32 shows the velocity vector diagram. Fig. 33 shows the close up view of the velocity vector diagram. Air flows smoothly and exhausts through the jets as shown in Fig. 33.



(a) Height=0.875 cm (b) Height=1.86 cm (c) Height=3.11 cm



(d) Height =4.36 cm (f) Height=6.24 cm (g) Height=11.24 cm

Fig 31. Contour diagram for temperature

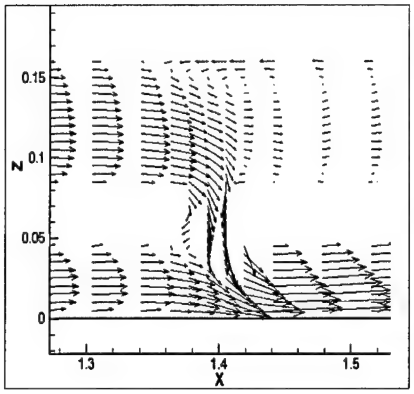


Figure 32. Velocity vector diagram

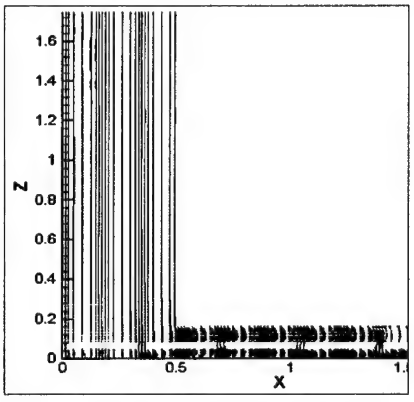


Figure 33. Close-up view

Height of the inlet jet(cm)	Temperature at the inlet jet	Temperature at the bottom
0.875	50	4.87
1.86	15	2.53
3.11	7.8	2.21
4.36	5.3	2.01
6.24	2.0	1.98
11.24	1.0	1.83

Table 5. Height and Temperature at the inlet jet

(e) Conclusion

The flow and heat transfer in the MEMS based air micro-jet array (MJA) impingement cooling device is computed by solving the incompressible Navier-Stokes (NS) equations. The flow equations are solved by finite difference procedure in a rectangular grid system. Steady state flow is reached by solving the temperature distribution. . The computed temperature distribution at the top of the bottom plate where the micro jets array, is compared with the experimental measurements of Leland et al. (1999). This goal was met and computational results were in good agreement with the experimental results of Leland et al. (1999). Application of geometry changes to the micro-jet array using the computational model led to increasing the cooling capacity of the array by 78%. A computational model was developed for two-dimensional compressible flow using the original micro-jet array. Then a three-dimensional model is being produced.

Task 3: Apply the Optimized MJA Device In An Application

Task 3: This task is to select, design, fabricate and implement an appropriate heat source to demonstrate workability of MJA test structures. This task is being performed by Dr. Ajay Malshe and his graduate students, Jedediah Young (1 year), K. Sharif (6 months) and D. Deshpande (1 year) The main sub-tasks are:

- Selection and design of the thin chip heat source on flex substrate
- Fabrication and testing of the thin chip heat source on flex substrate
- Fabrication of the setup integrating the thin chip heat source on flex substrate with the microjet array assembly
- Implementation and Testing of the above assembly

Introduction and Background:

I. Selection of the Heat Source:

Based upon previous work, the Microjet array (MJA) has the ability to cool devices with a very high efficiency [3.11,3.22]. The selected candidate for the heat source - paper thin IC (50-80 μm thin) devices and related packages are at the forefront of the investigation and are of immense importance for achieving high density electronics for conformal as well as non conformal electronics, particularly for strategic air-borne applications. Efficient thermal management of these devices is at the backbone of their reliability. Paper-thin ICs are considered to be a new paradigm globally as well as in the Co-PI's (APM) research group for the realization of advanced system-in-a-package (SIP) and wafer-level and chip-scale packaging of MEMS and related micro systems [3.3,3.4]. In light of these issues, paper-thin silicon ICs on flexible substrates were chosen as the heat source. As will be discussed further, the flex substrate used had thermal vias drilled in it and filled with copper. The thermal vias are expected to enhance the heat transfer of the system and aid in effective cooling of the ICs. This is analogous to the MJAs that will be used to cool the ICs, since both are vertical structures with different dielectric constants, and are supposed to enhance the cooling of the IC by carrying away the heat generated. A comparative study of these two cooling structures will be made – one study with the vias and bottom cooling using a fan, and the other with the vias and the MJAs for bottom cooling. The inferences will be summarized for future reference.

II. Introduction to paper-thin ICs on a flex and Overview:

The main driving factor currentl in force in the electronics industry to increase the density of the devices per unit area and per unit volume. In addition, current packaging trends require the chip thickness to be reduced. The diameter of the wafers varies directly in proportion with their thickness. Hence, wafer thinning is needed to

fit active chips into thin packages. Thin chips are being used in such packages as Ball Grid Arrays (BGAs), MCMs, Smart Card, Chip Scale Packages (CSPs), etc. Some of the applications of thinned chips are memory cards, smaller disk drives, cellular phones, portable electronics, and micro electromechanical systems (MEMS).

Several advantages can be obtained from thin chips. They require less space, allow more functionality per unit volume by stacking, increase thermal performance by improving power dissipation, etc, resulting in a more reliable device. They also allow for a mechanically flexible device, which can conform to a curved surface, especially in aerospace applications.

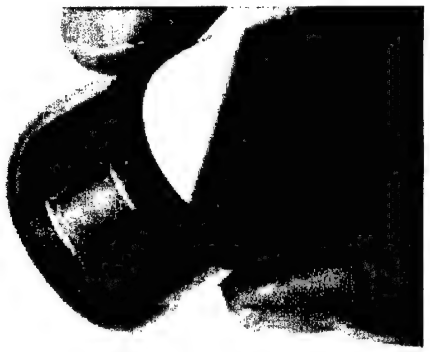


Figure 34: Bent Si thin chip, thinned by backside grinding, on Kapton® (APM's lab).

The resistance of heat flow through a material is a function of the distance the heat must travel (similar to electrical resistance in a wire). By thinning the chips, the resistance to heat flow through the chip is reduced. Also, this puts the source of the heat generation closer to heat sinks. With enhanced thermal performance, the chip can function on higher levels of power for better performance. However, when mounted on a flexible substrate such a polymer (Figure34; Kapton®, BCB, liquid crystal polymer- LCP, etc.), its poor thermal conductivity will be a bottleneck for the thermal management of the chips. Thus, integration of MJA can be an excellent combinatorial approach for thin chip silicon packages.

Further, reducing chip thickness helps to relieve stress induced on a chip while it is packaged. By thinning the chip, the distance from the top (or bottom) of the chip to the neutral axis is reduced. This allows for increased flexibility of the chip. Since the thinner chip has more flexibility, it is able to withstand higher coefficients of thermal expansion (CTE) mismatch. Another cause of stress failure is the solder ball joint in flip chip configurations. Again, because of the chip's flexibility, it is able to relieve stress that could cause cracking in the solder ball and the chip itself.

The thickness of the wafer has come down from about 500 microns (~20 mils) to the current methods, which can yield thicknesses as low as 15 microns.

The following discussion highlights the fabrication of the test structure and related technical approach for measuring thermal performance with the MJA. Application of MJA to these structures will be the remaining portion of this task.

III. Technical Approach and Results:

III.a Thinning of the ICs

The two methods used in this work for thinning are atmospheric downstream plasma (ADP) etch by TruSi Technologies, Sunnyvale, CA and backside grinding and polishing by Irvine Sensor, Irvine, CA. Each method was used to thin a 5 inch PST2-03 Thermally Sensitive Test Heater Die wafer from Delco Electronics. [More related description of the die could be found in the next section.] Figure 35 shows the thinned

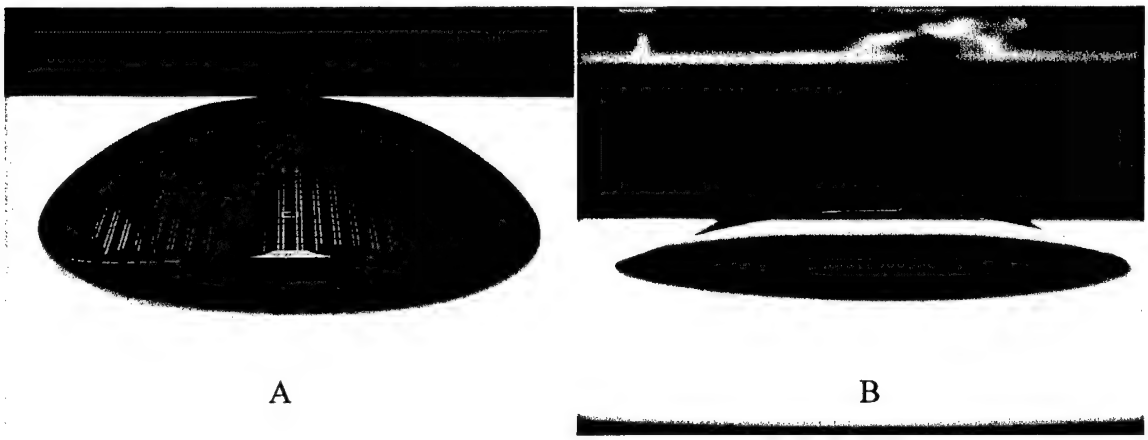


Figure35: (A) Thinned wafer after plasma etch, and (B) side view of bowed wafer.

wafers after the ADP processing.

These chips have been analyzed for chemo-mechanical analysis using various analytical techniques [3.5,3.6]. The purpose of the material analysis was to compare the effects that the two thinning processes have on the backside of a silicon wafer and then to compare this to an unprocessed wafer. The silicon wafers used were the PST2 Thermally Sensitive Test Heater Die wafers from Delco Electronics. The wafers are grown with a crystal orientation of <111> off 4.0 ± .5° towards the <110> plane. Once the silicon is cut into wafers, the backside is uniformly chemically etched. As mentioned, the two thinning methods studied are plasma etch and grinding-polishing. In this study, the wire bond and flip chip wafers were thinned to an approximate thickness of 50 microns. The characteristics that were studied were surface roughness and surface morphology using a Dimension 3000 atomic force microscope (AFM), Knoop microhardness with a Beuhler microhardness indenter and a Hitachi S-2300 scanning electron microscope (SEM), and residual stress with a Phillips X'Pert System X-ray diffraction. In order to simplify the material handling during the material analysis, the wafers were cut into individual dies.

Once the wafers were thinned and the chips were recovered, tests were performed to determine whether the chips performed as well as they did prior to

thinning. The chips were mounted to a metallized Kapton substrate using a Z-axis conductive epoxy.

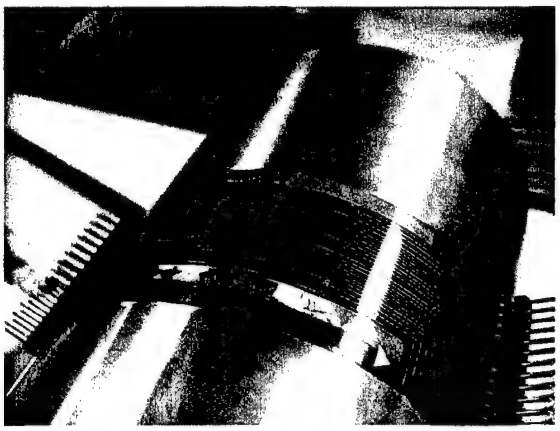


Figure 36: Test Circuit bent at 11.5 cm diameter of curvature

Z-conductive epoxy is ideal because is allows for a simple chip attachment, and it provides good support for the chip. During mechanical bending test, the attachment to Kapton® provided highly successful results for bending the circuit, as shown in Figure 35. The die in this picture was bent to a diameter of 11.5 cm. Further, bend testing under a uniaxial 4 lb load using a specially designed machine, demonstrated the mechanical integrity of the chip after 10,000 cycles. Electrical tests were performed to show that the thinning had no effect on the functionality of the chip. Electrical characterization of the die indicated that the thinning did not damage the die.

III.b Material Selection and Preparation of test structure for testing thermal management

This section will discuss the materials and system architecture used to assemble these systems. Due to the many potential uses of flexible electronics, this project does not apply to a single application of flexible systems - yet it creates a flexible system that allows the overall goals of this project to be accomplished. Material choice is key to obtaining a system that is flexible and is able to maximize power output. These materials are a thin silicon chip, a flexible substrate and an interface between the two that does not distort the flexing or heat transfer capabilities.

PST2 Thermally Sensitive Thin Chips-

The thin chips used were Delco Electronics' PST2 Thermally Sensitive Test Heater Die wafers. A heater die was chosen so that both electrical functionality and heat analysis could be tested. Although the silicon chip has been thinned, its bulk material properties do not change.

The PST2-03 chip is a heater die used to simulate and measure the power dissipation of active integrated circuits. The chip consists of two independent circuits: heating circuit and temperature sensing circuit. The heating circuit utilizes a 16-30 ohm

resistor as its heat source. The resistor is composed of Al/Cu/Si (98/1/1). By varying the current passing through the chip, and thus the voltage drop, the chip can be set to dissipate a desired power. The power dissipated depends on the effectiveness of the system's ability to transfer heat away from it. The heating circuit has two input/outputs (I/O) as shown in Figure 37.

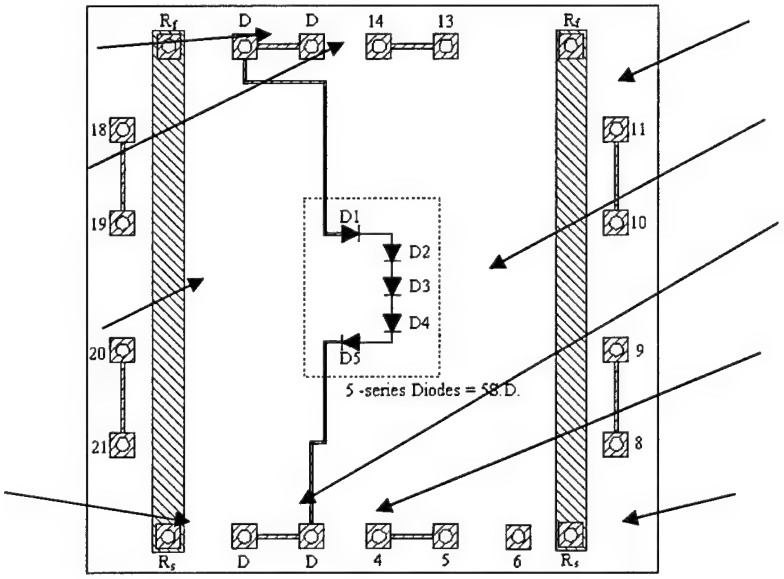


Figure 37: Schematic of PST2-03 Thermally Sensitive Test Die

As shown above, the heating resistors lie along the side of the chip. The current passes through the chip via the heating current I/O, and when the heating strips are activated, they perform in such as was as to simulate a uniform heat flux on the top of the chip. Note that either the two heating current I/O at the top or bottom of the resistors can be used to complete the circuit.

The sensing circuit consists of a five chain diode series. A 100 A current is required to pass through the chain in order for it to be activated. As the chip heats up, the resistance of the diode chain increases. This results in a change in voltage drop across the chain. The voltage drop across the diode is correlated to the chip's temperature. Physically, the chip measures 0.150 x 0.150 in^2 (3.8 x 3.8 mm^2) with a thickness of 50 - 80 microns. The metal layer that makes up the resistor is approximately 24,000 Ω. The entire chip is covered with a 10,000 Ω nitride passivation layer. The dimensions of the pads are shown in the following Figure 38.

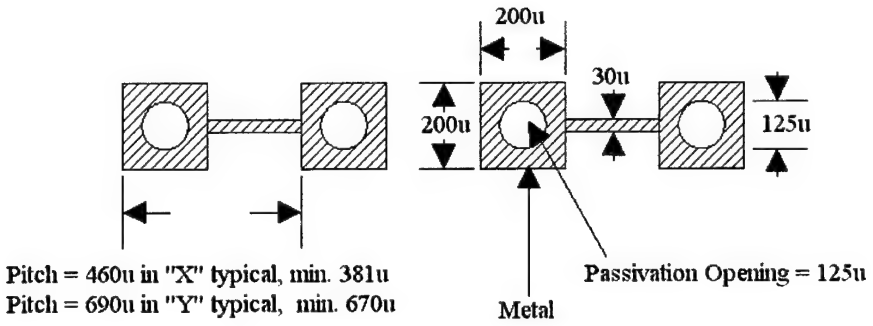


Figure 38: Schematic of PST2-03 I/O Bond Pads

Adhesive Interface-

In order to maintain the mechanical flexibility of the thin chip system, the interface material between the thin chip and substrate must be flexible. To achieve this, a double-sided thermally conductive tape was chosen. The conventional method of attaching a wire bond chip to its substrate is by the use of a thermally conductive epoxy. Also, the conventional means of attaching a flip chip IC to its substrate is by the use of solder balls for electrical connection and an underfill for the mechanical and thermal bond. Although these interface materials are very reliable and effective, they are also very rigid. This rigidity can cause unnecessary stress in the IC itself if attempting to flex. This characteristic is not desired for a truly flexible system. Thermally and electrically conductive tapes can replace these traditional materials in a flexible system to decrease these induced stresses. Thermally conductive tapes for wire bond configurations allow reliable attachment and comparable thermal efficiency, yet allows flexibility. A number of tapes were explored, and 3M Thermally Conductive Adhesive Transfer Tape 9890 was used in final package fabrication.

The z-axis electrically conductive tape (3M) allows reliable attachment, thermally efficiency, and flexibility, yet it also allows for an electrical connection. A paper by Kevin Y. Chen, et al, "Ultra-Thin Electronic Device Package," describes in detail how z-axis conductive tapes can be used. Most ICs contain a passivation layer over the chip's circuitry with openings for the I/Os. One key goal in their work was to make the electrical connection between the circuit and recessed Al pad. According to the paper, this was achieved by gold bumping the Al pad. An attempt was made to reproduce their work in this project, but there was no way to bump the PST2 chips. However, other attempts were made to attach a flip chip configuration IC. This will be explored in the future.

Substrate (flex and vias)-

The substrate plays a very important role in the package. It must carry the circuitry for electrical functionality, must have the ability to transfer heat away from the thin chips, and must be mechanically flexible for the systems' conformability. To satisfy these requirements, a double-sided copper coated, polyimide film was used. The copper can be patterned by photolithography to create the electrical circuit. Copper is a good material because of its ability to adhere to the polyimide through an adhesion layer, and due to its electrical and thermal conduction properties. The film is

mechanically flexible, and by the use of laser drilling, micro vias can be made in the material for vertical thermal conduction. Sheldahl of Littleton, CO, manufactured the flex chosen. Sheldahl uses a laser drilling process to create vias. The vias are conical in shape with a 60 μm entrance diameter and a 25 μm exit diameter. The minimum via pitch with this size via is 200 μm center to center.

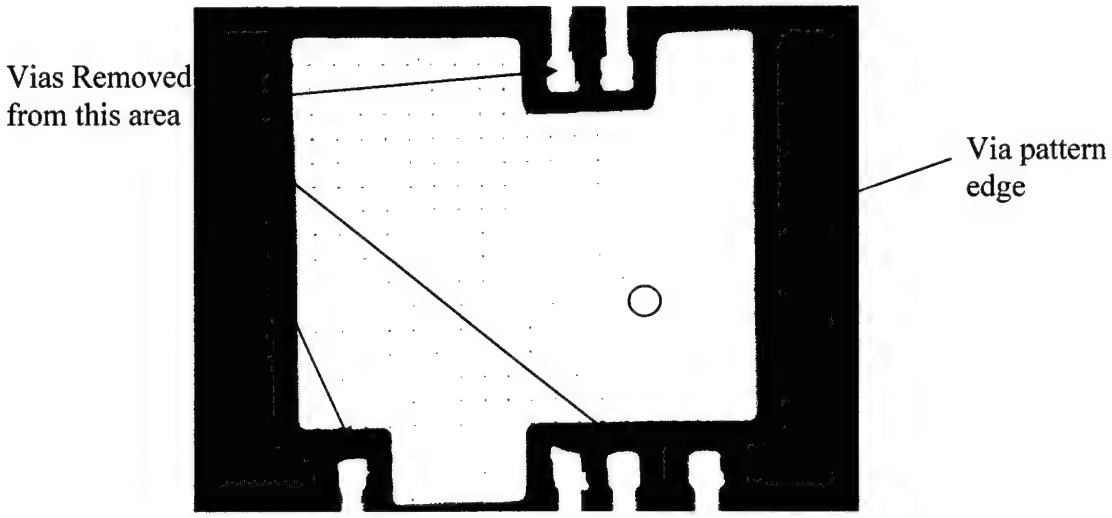


Figure 39: Chip scale via pattern and copper chip pad.

The via pattern design was based on the ability to use it for both wire bond and flip chip circuitry. The chip scale via pattern is 19x19 array of vias with sections of vias removed to accommodate flip chip circuitry. Figure 39 shows the via pattern design with the flip chip circuitry. For a wire bond circuit, the leads are moved back past the edge of the via pattern to allow room for the face up configuration of the die.

Once the vias are created, a plating process is used to fill the vias, as well as, to coat the polyimide. These vias are integrated to enhance uniform thermal accessibility of the thin heater chips to the MJA heat sink. Further, in order to achieve the copper plating, a chromium layer is first applied to both sides of the polyimide. This chromium layer is only a few microns thick, and acts as the adhesion layer between the copper and polyimide. Once the chromium is on the flex, copper can then be plated. The plated copper is 15 m on both sides. Due to the plating process, the via dimensions described above are the largest possible that can be filled. In addition to the laser drilled vias, tooling holes are also created to help orient the location of the vias for photolithography processing.

System Architecture-

The system architecture is the build up of materials in the flexible system. This section explains in detail how all these materials fit together and dimensions of certain components.

Layers-

The system architecture of the flexible electronic system consists of a 3x3 array of thin chips spaced 5 mm apart. Once the substrate completes the fabrication process, gold circuitry and copper chip pads remain. The first layer of the system is a thin Si chip. The second layer is the 3M thermally conductive tape, which is used to attach the chip the third layer, the copper chip pad.

Also on the third layer is the three-layered circuitry. The bottom layer is the 15 μm copper plated by Sheldahl. Plated on the top of this is a 1 μm layer of nickel, which acts as an adhesion layer for the top layer of gold. The gold layer is 5 m, which is used for two reasons. The gold keeps the copper from oxidizing, and it is also a good electrical conductor. The width of the circuit leads is about 0.5 mm. The next layer after the copper chip pad, is the polyimide substrate. This layer may also contain the vias. For comparison purposes, some circuits were, of course, made without vias in the substrate. Figure 40 shows the top layers of the system.

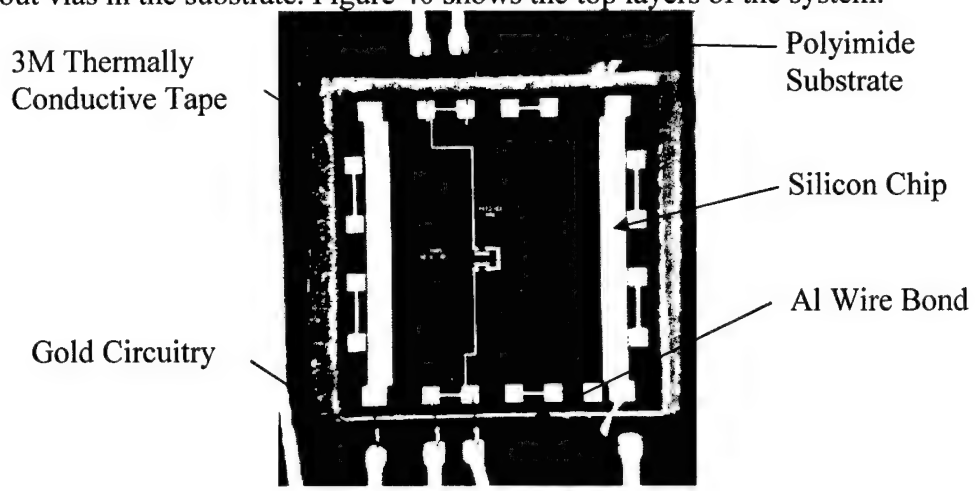


Figure 40: Top layers of the flexible system.

The fifth layer of backside copper adjoins the substrate layer. This backside copper acts as a heat spreader for enhanced heat transfer to the MJA heat sink. To ensure a flat contact with the surface of the heat sink and the backside of the circuit, a very thin layer of thermal grease is applied to the face of the heat sink. The final layer is, of course, the Microjet array heat sink.

Circuit Scale Via Pattern-

The circuit scale via pattern is common to all configurations. This pattern of vias consists of a 3x3 array of chip scale vias. The pattern was designed with the aim of maximizing the processed surface area to created two bottom cooled circuit configuration and one edge cooled circuit configuration. In doing so, the chip scale via patters were set 5 mm apart. This allowed enough room for the three circuits, all the necessary electrical lead, and the surface mount devices. This circuit scale via pattern also defines the position of the heater die. In addition to the pattern itself, other pattern design parameters included the theta orientation of the circuit with respect to the flat on the processing substrate and reference tooling holes made in the flex at the time of manufacturing.

IV Results of cooling with vias and fans

Description

The paper thin ICs were attached to the flex polyimide substrate and cooled without using the MJAs as a first step in the research. Figure 41 shows a map of the chip array, with the chips numbered for ease of understanding. The chips were cooled from the bottom using a 710F Fan Sink for AMD microprocessors manufactured by Wakefield Engineering. This is an aluminum fin sink with an overall thermal efficiency of 1.17 °C/W. Attached to the sink is a 12 V DC fan for forced convection transfer to the surrounding environment. This sink is a typical off the shelf component.

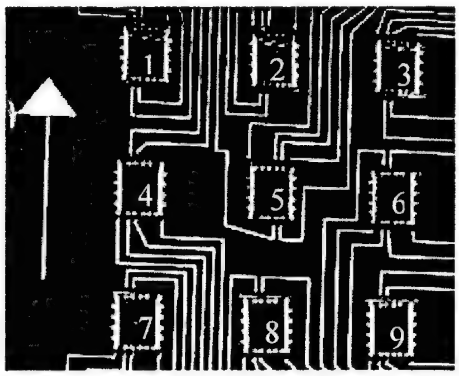


Figure 41: Chip Array Map

Figure 42 shows the performance of the chips at different power levels without cooling and Figure 43 shows the temperature across the chips when they were cooled using the fan from the bottom. Chip 9 was defective; hence its results are not included. The results obtained for the bottom cooled ICs using a fan are shown in Figure 44.

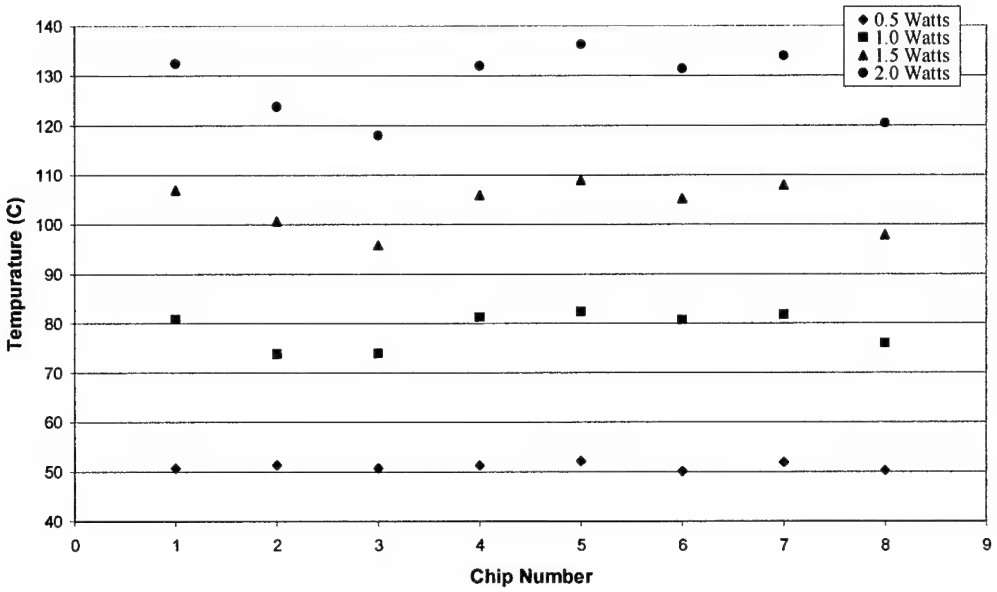


Figure 42: Thermal Results for Bottom-Cooled, No Vias Circuit Array

As seen from the figures, for the data for the high power dissipation (2 W), the ΔT between the chips are relatively large. This indicates that heat transfer occurs vertically through the system. If horizontal heat transfer were the dominating mode of transfer, the ΔT between chips would be much smaller.

This circuit also has bad data points. It was anticipated that this system would have a symmetrical thermal profile, but chip 3 appears to be at a higher than expected temperature. At a dissipation of 2 W, this point actually gets hotter than the center chip, chip 5. This problem also involves the adjacent chips. It causes them to be hotter, and thus, creates an unexpected profile. Although this is a bad point, it can not be excluded from the data because of its role in the make up of the thermal profile.

Chip 7 also adds to the misrepresentation of the thermal profile. The power circuit of chip 7 was not functioning properly, so any power dissipation that should have occurred did not occur. One assumption made is that if this chip was activated, it would affect the temperature of the surrounding chips, and chip 5 could possibly be the hottest chip.

The reason for bad points stems from the thermal performance of the system. It is apparent from the known profile that the dominating mode of heat transfer is vertically through the system. Hence, vertical transfer would be one of the main reasons for a profile irregularity. The decrease in vertical heat transfer can only be caused by an increase in thermal resistance. This increase in thermal resistance vertically under some chips and not others is most likely caused from a non-flat backside of the circuit. In other words, the backside of the circuit is not flush or in contact with the top of the heat sink. A thin layer of thermal grease was used to adhere the circuit to the heat sink. Too little thermal grease under chip 3 could cause it to not be in contact with the heat sink. Hence, it is imperative to ensure that in any

flexible circuit application where bottom cooling is to be used that the backside of the circuit be in full contact with the heat sink.

Results and Discussion

In comparing the two bottom-cooled circuits, one of the main goals of this work can be proven. The thermal vias do add to the thermal performance, and for a given

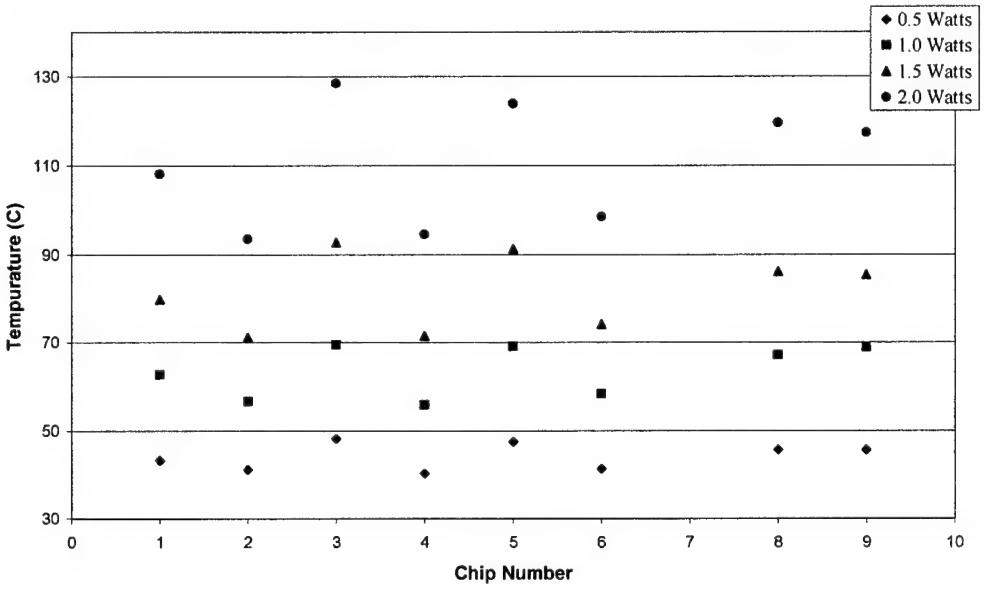


Figure 43: Thermal Results for Bottom-Cooled with Vias Circuit Array

operating temperature, the system with the thermal vias can operate at a higher power level. As shown in the results, the fact the ΔT between chips in the system with thermal vias is larger than the ΔT between chip of the no via system shows that the thermal vias do play an important role in the thermal performance and vertical heat transfer.

The next step in this research would be to compare these results with the IC performance using MJAs as the cooling mechanism. This proposed research will be discussed in the next section.

V: Ongoing Research for Future work:

V A: Integration of the Microjet Arrays with the Flex ICs

The design and fabrication of the MJAs has been described in detail elsewhere [1,2]. The MJAs will be fabricated in silicon and in Low Temperature Cofired Ceramic (LTCC). An aluminum heat sink will be integrated into the MJA assembly to enhance the heat conduction away from the ICs. Since the MJAs are fabricated out of silicon or LTCC, both of which are not good conductors of heat, the addition of the aluminum heat sink is expected to enhance the heat transfer. An image of a representative heat sink is shown in Figure 8.

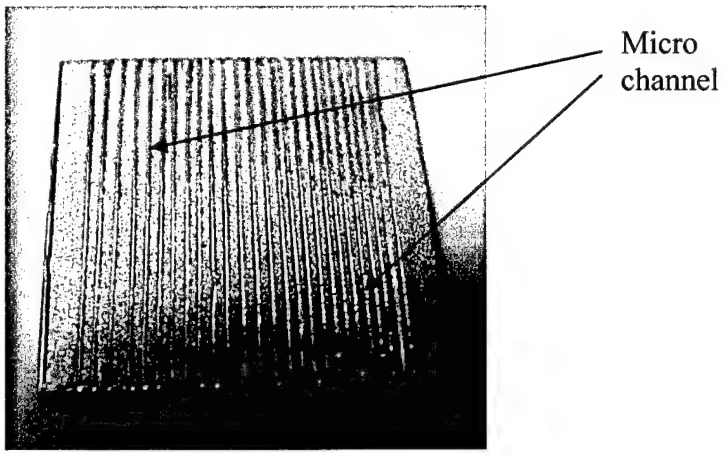


Figure 44: Image of the aluminum heat sink with the micro channels.

Microchannels will be fabricated on the back side of the heat sink. The pressurized air coming out of the microjets will impinge on these microchannels. The other side will be attached to the bottom of the flex substrate using a thermally conductive epoxy. A schematic image of the whole structure is shown in Figure 44.

The basic structure of the MJA is the same, with the addition of the aluminum heat sink added to the assembly. This will be bonded to the MJA using thermally conductive epoxy. The air will come from the top, flow through the plenum cover and the plenum, pass through the microjets and then impinge on the microchannels provided on the aluminum heat sink to carry heat away. The microchannels have been provided to increase the surface area in contact with the air flow, to enhance the heat transfer. The back side of the aluminum heat sink will be bonded to the polyimide substrate. The flex ICs will be bonded on the other side of the substrate. The vias provided in the substrate will aid in transferring the generated heat away from the ICs.

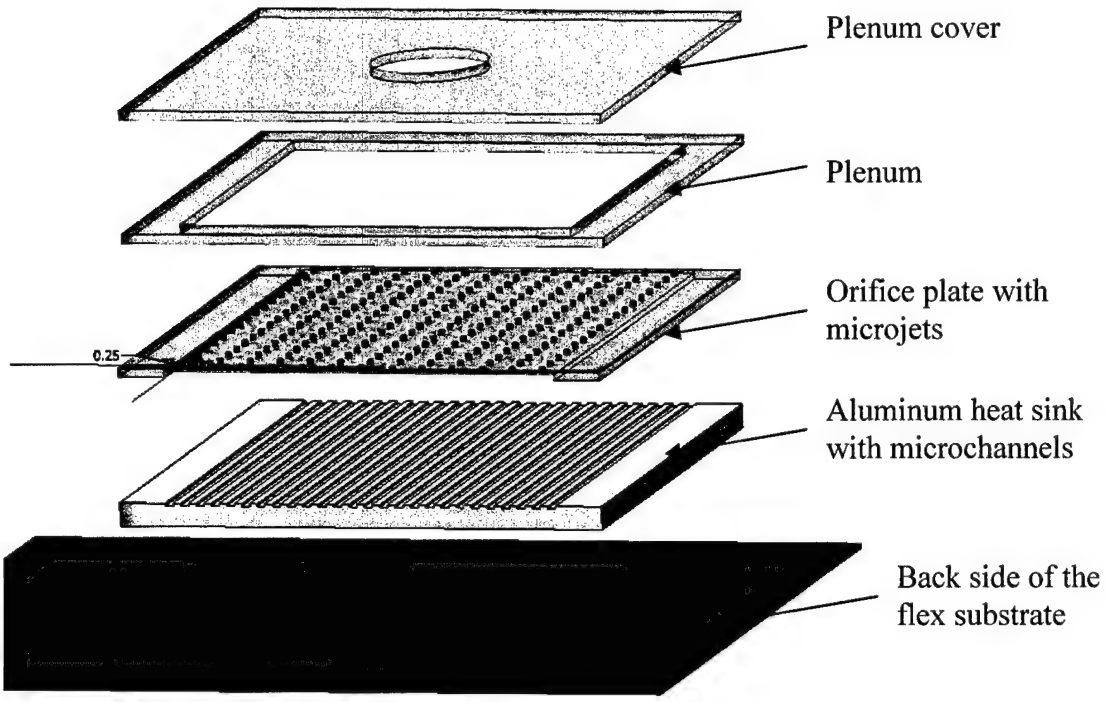


Figure 45 Schematic image of the microjet array assembly with the flex substrate.

The side of the aluminum heat sink that is to be attached to the substrate will be sand-blasted to increase the surface roughness, so as to ensure a better bonding between the two. The aluminum heat sink will be bonded to the MJAs and the substrate using thermally conductive epoxy and/or adhesive tape. A preliminary test of this bonding was carried out. Figure 46 shows the cross-section of aluminum bonded to silicon and LTCC using a thermally conductive tape.

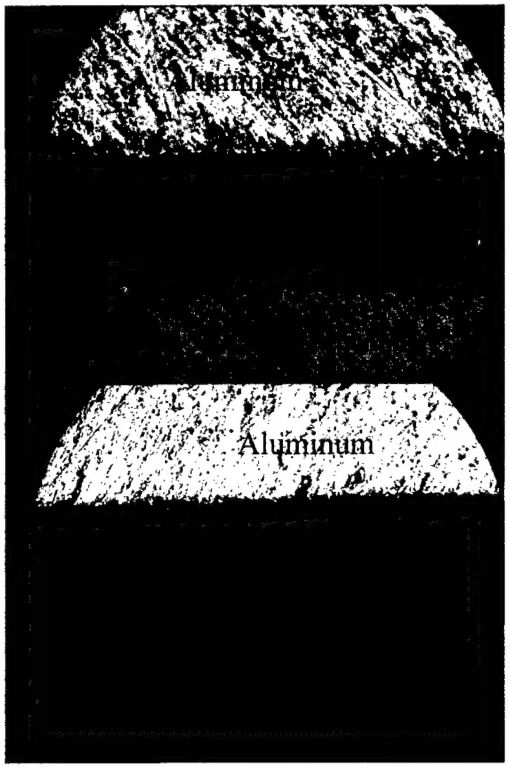


Figure 46 Cross-sections of bonding between aluminum, silicon and LTCC.

The figure shows that the bonds between aluminum and silicon and aluminum and LTCC are uniform and solid. Pull tests were performed on similar samples. The strength of the bonds exceeded the limit of the test setup, indicating that the bond is very strong.

V B: Testing of the integrated assembly

After the MJA has been bonded with the polyimide substrate, the whole assembly will be enclosed in an airtight fixture, which will ensure that the pressurized air pumped through the MJA will not leak out. The performance of the assembly will be evaluated against different air flow rates. This performance will be compared to the heat removal from the ICs using a 710F Fan Sink for AMD microprocessors manufactured by Wakefield Engineering.

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[3.6] "Fabrication, Thermal Modeling, and Analysis of Very Thin Silicon Chips on Flex for Conformal Electronic Systems", Jedediah J Young, Ajay P Malshe, W.D. Brown, Electronics Packaging Session, IMECE 2003, Sponsored by ASME, Washington D.C., November 2003.

Personnel Support

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K. Saxena, Electrical Engineering Ph.D. 2004
Y. Jung, Civil Engineering Ph.D. 2004
Jedediah Young, Mechanical Engineering, MSME, 2003.
K. Sharif, Mechanical Engineering, MSME student
D. Despande, Mechanical Engineering, doctoral.

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